

Report on EUVL Mask Substrate Development: Low-Expansion Substrate Surface Finishing II

W. M. Tong, J. S. Taylor, S. D. Hector, M. Shell

December 8, 1999

U.S. Department of Energy

Lawrence
Livermore
National
Laboratory

DISCLAIMER

This document was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor the University of California nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or the University of California, and shall not be used for advertising or product endorsement purposes.

Work performed under the auspices of the U. S. Department of Energy by the University of California Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

This report has been reproduced
directly from the best available copy.

Available to DOE and DOE contractors from the
Office of Scientific and Technical Information
P.O. Box 62, Oak Ridge, TN 37831
Prices available from (423) 576-8401
<http://apollo.osti.gov/bridge/>

Available to the public from the
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Rd.,
Springfield, VA 22161
<http://www.ntis.gov/>

OR

Lawrence Livermore National Laboratory
Technical Information Department's Digital Library
<http://www.llnl.gov/tid/Library.html>



Report on EUVL mask substrate development: low-expansion substrate surface finishing II*

**William M. Tong, John S. Taylor
Lawrence Livermore National Laboratory**

**Scott D. Hector
Motorola (assigned to EUV LLC)
EUV Limited Liability Corp.**

**Melissa Shell
Intel Corp**

8 December 1999

***This report was written to satisfy deliverable 8.1.5 of International Sematech Project LITH-111 "EUV Lithography mask blank substrate development."**

1. Abstract

This report is a continuation of our assessment of the finishing of low thermal expansion material wafers obtained through three different commercial pathways.

This quarter we have patterned and printed a ULE[®] wafer (Rodel 1) and saw no difference between its images and those from silicon wafer substrates. This further demonstrated that ULE[®] can be used as the EUVL mask substrate material.

We have also evaluated substrates produced by three vendors: Hoya, General Optics, and Rodel. Consistent with our results reported last quarter, surface roughness of the bare substrates from all three companies does not depend on the position. For Hoya, the wafers it produced had a low roughness than those from last quarter. However, the cleanliness of the wafers needs to be improved. For General Optics, the wafer roughness has increased, and it was only able to deliver one wafer this quarter. General Optics will be replaced by Schott ML next quarter. For Rodel, one of its wafers (Rodel 1) that had been cleaned in-house showed excellent finishing and was selected to be patterned. We also observed that the sleeks on the substrates were smoothed by the ML coating. The other two Rodel wafers (Rodel 2 and Rodel 4) had too many defects and the roughness values derived from AFM are not reliable.

2. Introduction

EUVL is a leading candidate to be the Next Generation Lithography (NGL) currently proposed to be inserted at the 70nm node. One of the key differences between EUVL and conventional optical lithography is that EUVL employs light that is 13.4nm in wavelength. Since the EUVL mask is reflective and coated with Mo/Si multilayers (ML), its requirements and properties are have significant differences from today's photomask. Silicon wafers are used as the mask substrates for development purposes down to the 100nm node for their low defect levels and low roughness. Silicon, however, has a high thermal expansion coefficient that would cause an image placement distortion that exceeds the overlay-error budget allocated for the 70nm node and beyond. Hence, a Low-Thermal-Expansion Material (LTEM) will be required. Presently, the low-expansion-mask substrates are produced in the shape of a standard 200mm silicon wafer with a notch to minimize the cost for changing our infrastructure. However, a 152mm-square and 6.35mm-thick photomask

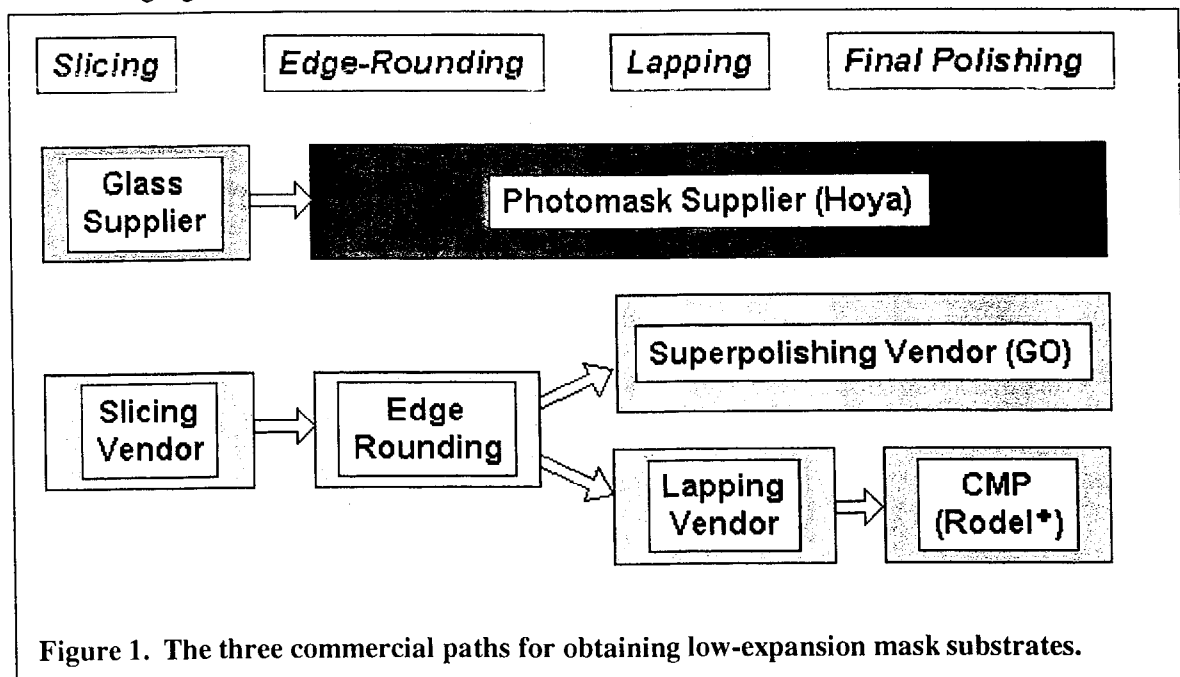


Figure 1. The three commercial paths for obtaining low-expansion mask substrates.

format will likely be adopted as the SEMI standard for production-class EUVL tools. The substrates evaluated in this report were all 200mm wafers.

Three commercial pathways for producing EUVL mask substrates are through a photomask supplier (Hoya), a superpolishing vendor (General Optics), and a CMP vendor (Rodel). We evaluated two wafers from Hoya, one from General Optics (GO), and three from Rodel. After these wafers were delivered, they were sent to an EUV LLC member company to be cleaned by distilled water with megasonic agitation and to receive a back-coating of Cr (for electrostatic chucking during ML-deposition). The wafers were then sent to Lawrence Livermore National Laboratory (LLNL), where they were inspected by AFM, coated with 41½ bilayers of Mo/Si, and reinspected by AFM. They were then sent to the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory to check for EUV reflectance. The reflectance spectrum of the sample was taken at the center of the sample. One of the wafers (Rodel 1) was chosen to be patterned and printed (details in section 4.1).

The EUV LLC/VNL infrastructure was converted from the 150mm wafer to the 200mm wafer format this quarter. The larger substrate presents an even greater challenge to our vendors, who have also been encouraged to vary their polishing parameters to optimize the finishing results. Thus this quarter's substrates have a larger variance in roughness than those reported in the last quarter.

Cleaning remains a challenge to the fabrication mask substrates. Although all six wafers were cleaned with distilled water and megasonic agitation, there were still too many defects to be measured by our light scattering tools (KLA-Tencor SP-1 and ADE Constellation) after a 70nm silicon coating. In the AFM scans of the four wafers that had not undergone thorough cleaning immediately after finishing (Hoya3, Hoya 4, Rodel 3 and Rodel 4), we still saw numerous defects even on a 10µm by 10µm scan of the AFM. The two wafers where the AFM observed no defects (GO 1 and Rodel 1) had been cleaned by the vendor in-house immediately after finishing. We believe our megasonic cleaning was ineffective because the wafers had been allowed to dry before.

Table 1: Names of the six wafers evaluated for this report

Supplier	Wafer Name
Hoya	Hoya 3, Hoya 4
General Optics	GO 1
Rodel	Rodel 1, Rodel 2, Rodel 4

3. Data analysis

The AFM data were collected by a DI 7000 located in a class-100 cleanroom at Lawrence Livermore National Laboratory (LLNL). The nominal sensitivity of the instrument for measuring surface roughness is 0.06-0.07nm rms. In the roughness calculation, most of the features that should be classified as defects were excluded. This is represented on the image by rectangular boxes with an "x" in the middle. The roughness value calculated from each AFM topograph is listed in Table 2 on p. 8.

Each wafer was scanned in two areas: the center and 80mm from center (Fig.2). For each area, two AFM scans of 10µm and 1µm were carried out, representing Mid Spatial Frequency Roughness (MSFR) and High Spatial Frequency Roughness (HSFR). The two regimes of roughness have different functional impact on lithography. MSFR leads to small angle scattering and may result in speckle, whereas HSFR scatters light out of the pupil and leads to a loss of effective multilayer reflectivity. The current mask substrate requirements for MSFR and HSFR are 0.20 and 0.15nm rms (updated 9/99), respectively. Consistent with our last report, we observed no finishing uniformity dependence on position for any of our substrates.

We will not be reporting the defect counts in this report. Our original plan was for the wafers to be coated with about 70nm of ion-sputtered silicon (at room temperature) and inspected with our KLA-Tencor light scattering tool. However, the number of defects was so large that it overwhelmed the buffer of the inspection tools (>32,000 defects). Furthermore, we ran the risk of contaminating the inspection tools which are an integral part of the low-defect mask blank production. Wafer cleaning will be key area of development for the next calendar year (to be addressed in the summary section).

The ML coating was carried out at the Ion Beam Sputtering Deposition (IBSD) tool located at Lawrence Livermore National Laboratory. Forty-one and a half Mo/Si ML were deposited onto the ULE substrates by ion sputtering. The mask blanks were sent to the Advanced Light Source (ALS) at Lawrence Berkeley National Laboratory for wavelength qualification.

For the printing demonstration, "Rodel 1" was chosen as the mask blank to be patterned and printed because it had the lowest roughness and lowest defect count. The details of the printing will be discussed in section 3.2.

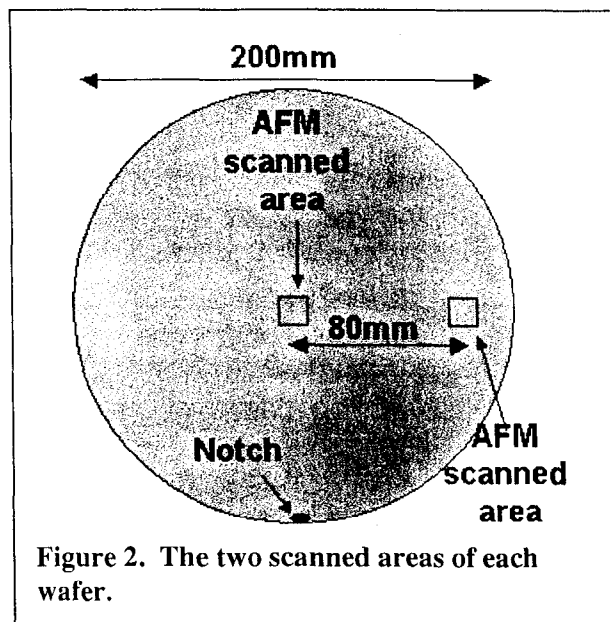
3.1.1 Hoya

The AFM topographs of the Hoya-lapped wafers are shown in Figures H in the appendix. The roughness data derived from those topographs are listed in Table 2. The average MSFR of the uncoated wafers (0.34nm rms) is similar to that of the two wafers from last quarter (0.35nm rms), but the HSFR has significantly improved from 0.35 to 0.28 nm rms.

Distinct defects were observed on both Hoya 3 and Hoya 4 wafers, but we do not believe they are uncorrectable problems. Both wafers were polished with colloidal silica but under slightly different conditions. On Hoya 3, the slurries have agglomerated into discrete islands. These islands on Hoya 3 are approximately 200-400nm wide and 20-30nm high. We believe these islands formed because the slurries were exposed to the incorrect pH environment either during polishing or during cleaning, and this will be corrected in the future. On Hoya 4, we observe on both 10 μ m scans semicircular streaks with radius of about 8 μ m. The height of these sleeks is about 5nm on Fig. H.4.0.10 and 2nm on Fig. H.4.80.10. These streaks have not been observed on other polished samples before and their origin is unclear. We do not believe they are reproducible events but will continue to monitor their reappearance in Hoya's future samples.

At Hoya Optics, no semiconductor-class cleaning tool was used. The substrates were dried and then sent to an EUV LLC company for cleaning with a semiconductor-class cleaning tool (distilled water and megasonic agitation) before being scanned with an AFM. The rudimentary cleaning immediately after finishing did not remove a significant number of defects. Once these defects were allowed to dry they became even more difficult to remove.

After ML-coating the surfaces of the wafers undergo significant changes. The AFM scan of the center area of Hoya 3 after coating (Fig. MH.3.0.10) shows that the underlying defects have caused ridges on the mulitlayer surfaces. These ridges range from 3-12nm in height and 100-700nm in width. This is consistent with observations by P. Mirkarmi that smoothing occurs on high aspect



ratio defects such as gold sphere of ~50nm in size, which have an aspect ratio of unity, but roughening may occur in lower aspect ratio defects such as the agglomerated island, which have aspect ratios of about 0.1 This reinforces our view that cleaning is a critical part of the finishing process. On Hoya 4, the coating appeared to have conformed to the substrate surface. This may be due to the fact that ML coating conditions are slightly different at the center of the substrate and at 80mm from the side substrates. Improving the uniformity of the ML coating is a focus of mask blank program for Y2000.

Both ML-coated wafers have EUV reflectance of about 54%, which is expected given the HSFR values at the center of the two substrates.

3.1.2. General Optics

GO is not a volume producer and was only able to deliver one ULE[®] wafer this quarter. (It will be replaced by Schott ML in the next quarter.) With approval from Sematech, the second wafer from GO was replaced with an additional wafer from Rodel. The eight AFM topographs of the GO-finished mask substrates are shown in Figures G of the appendix. The overall quality of the finishing of the bare substrates has deteriorated from that of the wafers produced by GO in the last quarter. Both the MSFR and HSFR increased from 0.22 and 0.21 nm rms in the last quarter to 0.24 and 0.38nm rms, respectively. Furthermore, we saw more pits and streaks on this quarter's wafer than on last quarter's. However, no particles were observed in the scanned areas, probably because GO cleans the surface thoroughly with surfactants and deionized water immediately after the wafer was finished. The wafer was further cleaned with megasonic agitation at the EUV LLC member company.

The ML coating significantly smoothed the surface, decreasing both the MSFR and HSFR to 0.16 and 0.14 nm rms, respectively. The low roughness of the coated surface also is probably the reason that this wafer has the highest reflectance of all samples.

3.1.3. Rodel

Rodel is a major supplier of slurries and pads for the optical finishing and chemical mechanical polishing (CMP) industries. Its laboratory is geared for developing CMP processes for the semiconductor industry. Rodel interacts closely with chipmakers, silicon wafer manufacturers, and photomask suppliers and therefore understands the importance of low defect levels and low surface roughness. All of Rodel's CMP operations and metrology are carried out in a cleanroom (class-100) and it possesses a comprehensive set of tools for cleaning, defect inspection, and surface finishing.

Because of EUV LLC/VNL scheduling and deadline pressure to coat and pattern these wafers, Rodel was only able to clean one (Rodel 1) of the three samples before delivery. Rodel 1 received a SC-1 clean by a semiconductor-class cleaning tool immediately after finishing, whereas Rodel 2 and Rodel 4 only received rudimentary cleaning. The difference between the samples can be easily told from the topographs. The subsequent cleaning at the EUV LLC company was insufficient for Rodel 2 and Rodel 4. This reinforces the view that cleaning immediately after finishing is crucial to producing low-defect surfaces. Rodel 4 was not scanned by the AFM before coating because the ISBD tool was about to become unavailable for three weeks for maintenance and the coating had to be done immediately. The large number of defects present on Rodel 3 also severely restricted our ability to measure the substrate surface topography and roughness. We therefore will concentrate our analysis below on Rodel 1.

The twenty AFM topographs of the Rodel-finished mask substrates are shown in Figures R of the appendix, and it was evident from the topographs that the Rodel substrates have the lowest roughness. The average MSFR and HSFR of Rodel 1 are 0.20 and 0.14nm rms, which are slightly

inferior to last quarter's values of 0.16 and 0.15nm rms, but they met our specifications. The sleeks on these wafers have an average depth of 0.37nm and a top width of 280nm. After ML-coating, the surface became rougher, with the average MSFR increasing from 0.20 to 0.26nm and the average HSFR increasing from 0.14 to 0.21nm rms. The AFM scans of the coated surfaces Figs. MR.1.0.10 and MR.1.80.10 show the sleeks have been further smoothed by the multilayers. These sleeks are not printable.

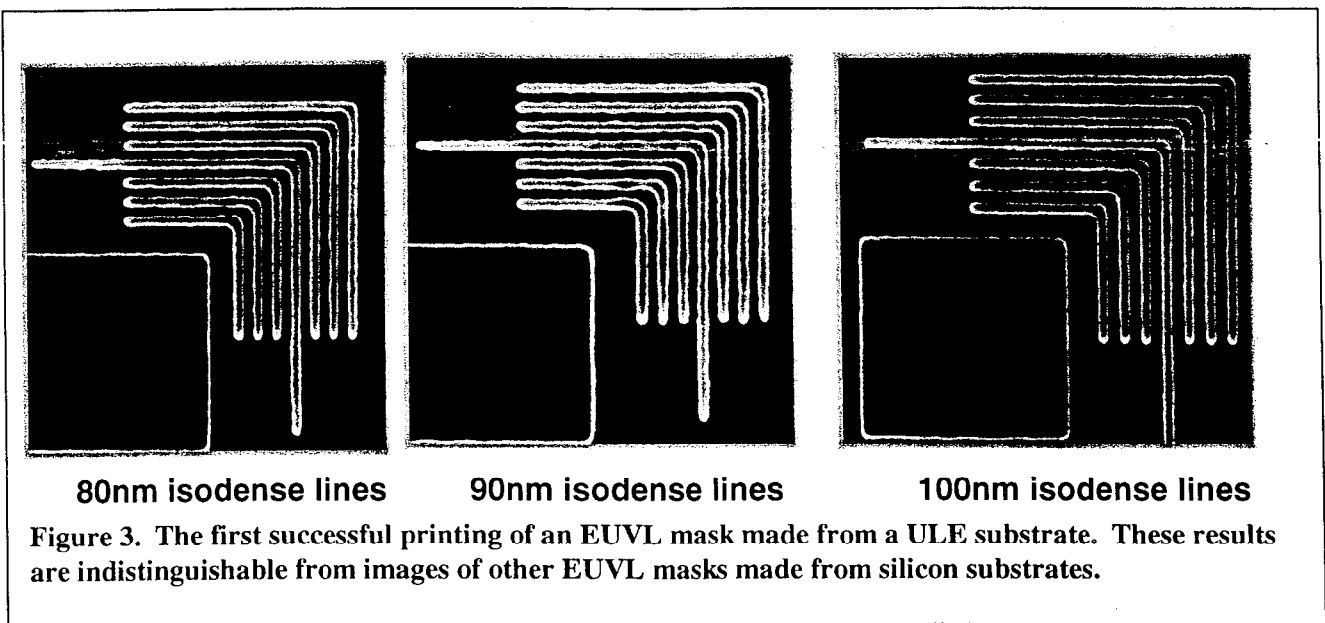
Rodel 1 had a reflectance of about 55%, which is slightly lower than what one would expect for substrates with MSFR and HSFR of 0.21 and 0.15nm rms. However, after the coating the MSFR and HSFR of the surface have increased to 0.30 and 0.26nm rms, respectively. This may be a factor in the expectedly low reflectance of Rodel 1. For Rodel 2 and Rodel 4, their reflectance values were low probably because of the high number of defects on the substrates.

3.2 Printing

Rodel 1 was selected as the wafer to be printed for its cleanliness and low roughness. The ML-coated wafer was sent to an EUV LLC company for patterning. The patterning steps are as follows.

1. Deposit 45nm of SiO₂ buffer layer by chemical vapor deposition.
2. Deposit 100nm of TiN absorber layer by plasma enhanced chemical vapor deposition.
3. Spincoat photoresist on wafer.
4. Pattern with DUV exposure stepper.
5. Strip photoresist with oxygen plasma.
6. Remove buffer layer with fluorine plasma.

The patterned mask was printed at Sandia National Laboratories with the 10x microstepper. The resultant images for 80, 90, and 100nm line pitches are shown in Figure 3. To within the repeatability of the microstepper, these images are indistinguishable from other images of EUVL masks made from silicon substrates. This demonstrates the ULE[®] can be used as substrate material for EUVL mask production.



4. Summary

This report is a continuation of our assessment of the finishing of LTEM wafers obtained through three different commercial pathways. For Hoya, the roughness of the wafers it produced improved from last quarter. However, the cleanliness of the wafers needs to be improved. For GO, the wafer finishing quality has declined, and it was only able to deliver one wafer this quarter. For Rodel, one of its wafers (Rodel 1) that had been cleaned in-house showed excellent finishing and was selected to be patterned. We also observed that the slicks on the substrates have been smoothed by the ML coating. The other two wafers (Rodel 2 and Rodel 4) had too many defects and the roughness values derived from AFM are not reliable.

The printed images from Rodel 1 were indistinguishable from other images derived from silicon wafer substrates. This demonstrates that ULE[®] can be used as the EUVL mask substrate material.

It is clear that cleaning is an area that requires development. We observed that cleaning the wafers immediately after finishing is necessary to reduce the defects. Otherwise, the slurries will become dried and bound to the substrate. A one-step cleaning with distilled water and megasonic agitation is likely to be insufficient. Furthermore, ULE[®] and silicon have different surface chemistries which would require the use of different cleaning reagents.

The wafers evaluated in this report could not be inspected by the light scattering tools (KLA-Tencor SP-1 and ADE Constellation) because of the high defect counts, which saturated the buffer. Our goal will be to obtain substrates with a low enough defect count to allow them to be inspected.

Our plan for the next calendar year is as follows.

1. Replace GO with a photomask company, Schott ML. GO's low volume manufacturing was only able to deliver one wafer and its finishing is not superior those of the other vendors'. Schott ML is the main photomask supplier from Europe that has inspection and clean infrastructures. Both Schott ML and Hoya have inspection and cleaning in their photomask production facilities. This will allow us to evaluate the state of the art in photomask finishing.
2. Producing clean substrates requires inspection. A limited number of LTEM photomasks and wafers will be inspected by KLA-Tencor with its development mask inspection tool. The results will provide feedback to the finishing vendors.
3. Substrates made of Zerodur[®], which is low-expansion glass-ceramic, will be produced for the first time. Schott ML will supply both Zerodur[®] and ULE[®] photomask substrates every quarter for our evaluation.
4. The clean and inspection infrastructure of the silicon wafer industry still produces substrates with superior defect counts to the photomask industry and may be leveraged to produce low-defect substrates. We will explore the viability of applying an amorphous silicon coating of about 1 μm on the LTEM substrates, which can cover up discrete defects and allow access to the more sophisticated silicon cleaning tools and recipes for defect removal. The silicon coating will be repolished and cleaned by Rodel, which has vast experience in finishing process development for silicon.

5. Acknowledgment

The authors acknowledge Cindy Larson and Chris Walton of LLNL for collecting all the AFM data, Patrick Kearney and Joel Bowers for ML coating the wafers, and John Goldsmith, Donna O'Connell and Daniel Falk of Sandia National Laboratories (Livermore) for the printing of the patterned mask. We also would like to thank James Wasson and Pawitter Mangat of Motorola and Guojing Zhang of Intel for help in processing the wafers. This work was performed under the

auspices of the U. S. Department of Energy by the Lawrence Livermore National Laboratory under contract W-7405-ENG-48. Funding was provided by the Extreme Ultraviolet Limited Liability Corporation under a Cooperative Research and Development Agreement. Additional funding was provided by International Sematech under Project no. LITH-111 "EUV Lithography mask blank substrate development."

Table 2. Surface roughness derived from AFM topographic data of mask substrates finished by the three vendors. Rodel 4 was not prescanned by AFM before coating because of scheduling conflict between AFM and LDD tool. An asterisk (*) denotes the roughness count may not be accurate due to the influence of discrete defects.

	ROUGHNESS, CENTER (in nm rms)				ROUGHNESS, 80MM FROM CENTER (in nm rms)				EUV REFLECTANCE (CENTER)		NOTES
	Pre-coating (nm rms)		Post-coating (nm rms)		Pre-coating (nm rms)		Post-coating (nm rms)		Percent Reflectance (%)	Peak Wavelength (nm)	
	MSFR	HSFR	MSFR	HSFR	MSFR	HSFR	MSFR	HSFR			
HOYA 3	0.32	0.25	0.39	0.27	0.32	0.26	0.29	0.34	53.5	13.5	Agglomeration of slurries was observed.
HOYA 4	0.33	0.29	0.34	0.30	0.38	0.29	0.27	0.23	54.3	13.5	Circular ridges of 2-5nm in height were observed
GO 1	0.19	0.38	0.16	0.14	0.29	0.38	0.16	0.14	56.7	13.5	Larger value of HSFR than MSFR
RODEL 1	0.21	0.15	0.30	0.26	0.19	0.13	0.22	0.16	55.1	13.4	Best overall substrates. Used for printing.
RODEL 2	0.47*	0.33*	0.42*	0.21*	0.65*	0.44*	0.42*	0.19*	51.5	13.4	High defect count. Wafer had been allowed to dry before thorough cleaning.
RODEL 4	NA	NA	0.45	0.32	NA	NA	0.39	0.43	52.8	13.5	Wafer not scanned prior to ML coating because the ISBD tool was to become unavailable for 3 weeks.

Appendix: AFM topographs and reflectance curve of the wafers

Six wafers from three companies were evaluated. Two areas on each wafer was scanned at two scan sizes (10 μ m and 1 μ m) before and after coating, bringing the total number of scans to forty-eight. It is important to note that the AFM scans carried out in the same nominal area were not necessarily done in exactly the same area, as the cross-registration for the AFM is too time-consuming to be carried out for this study. The reflectance for each wafer was measured at the center of each wafer.

The figures in this section are organized as follows.

- The first letters of the figure name denotes the company (H for Hoya, G for General Optics, R for Rodel) and whether the surface was multilayered coated (M for multilayer coated).
- The first numeral corresponds to the wafer number.
- The second numeral refers to the region where the scan was made (“0” refers to center, “80” refers to 80mm from center, see also Figure 2).
- The third numeral refers to the scan size (10 for 10 μ m and 1 for 1 μ m scans).
- An asterisk (*) on the roughness value denotes the high defect count on the substrate has introduced large uncertainty to the number.
- Note that Rodel 4 had not been scanned with an AFM prior to ML-coating because of scheduling constraints.

For example, “Figure MR.3.80.1” means the scan was taken from a multilayer coated Rodel wafer 3, 80mm from the center, and with a scan size of 1 μ m.

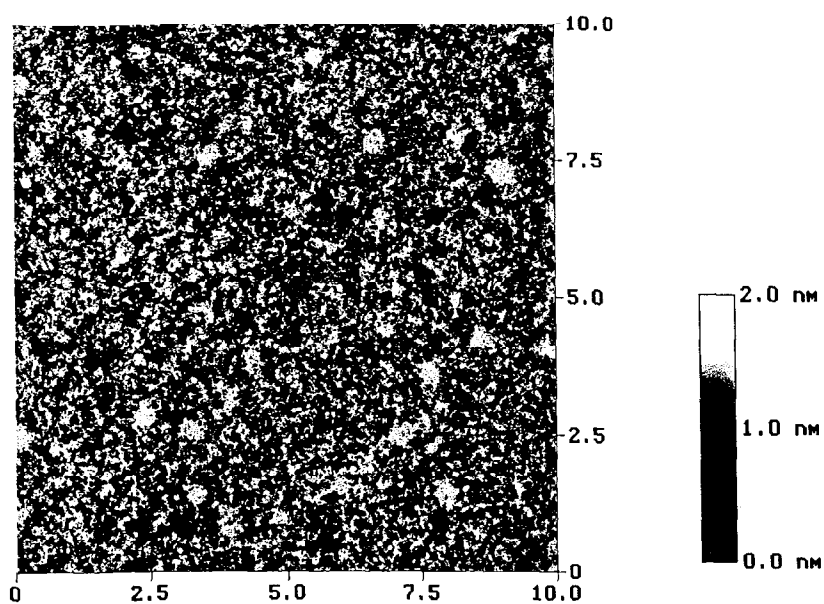


Figure H.3.0.10: 10 μ m scan, Hoya ULE wafer no.3, center. MSFR = 0.32 rms. The defects, which been excluded from the roughness calculation, are likely to be agglomerated slurries. These islands have dimensions of 200-400nm in width and 20-30nm in height.

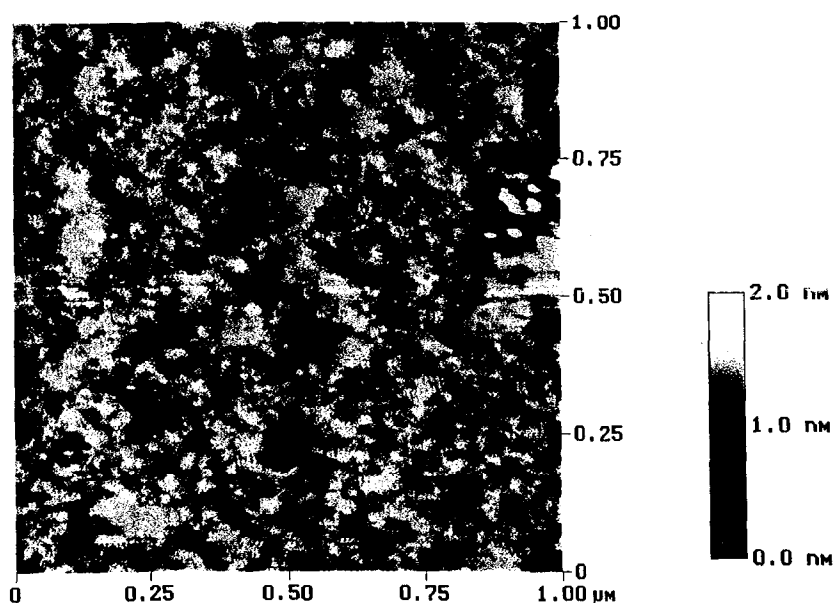


Figure H.3.0.1: 1 μ m scan, Hoya ULE wafer no.3, center. HSFR = 0.25nm rms. The defect on the right corner was excluded from the roughness calculation.

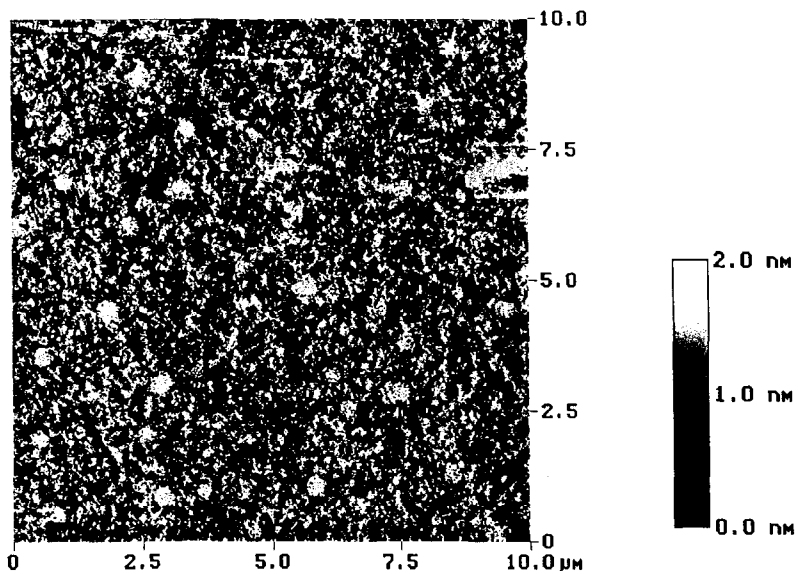


Figure H.3.80.10: 10μm scan, Hoya ULE wafer no.3, 80mm from center. MSFR = 0.32nm rms.

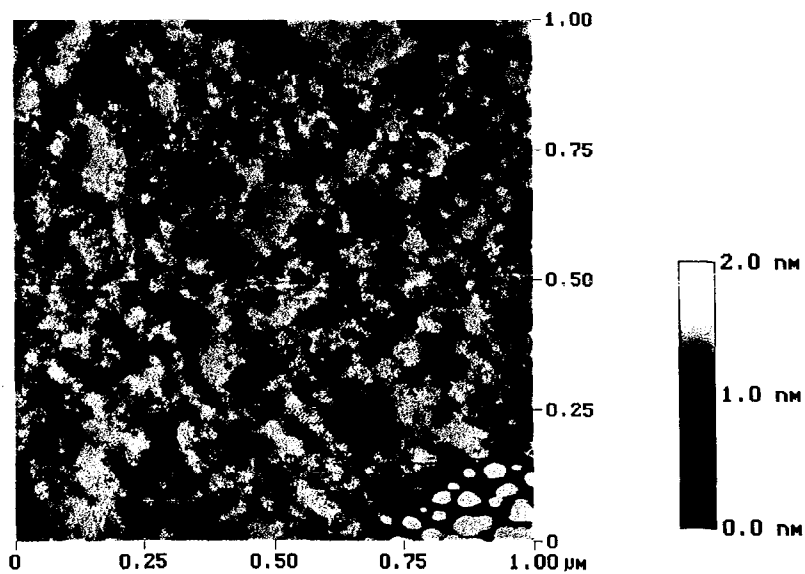


Figure H.3.80.1: 1μm scan, Hoya ULE wafer no.3, 80mm from center. HSFR = 0.26nm rms. The defect on the lower right corner was excluded from the roughness calculation.

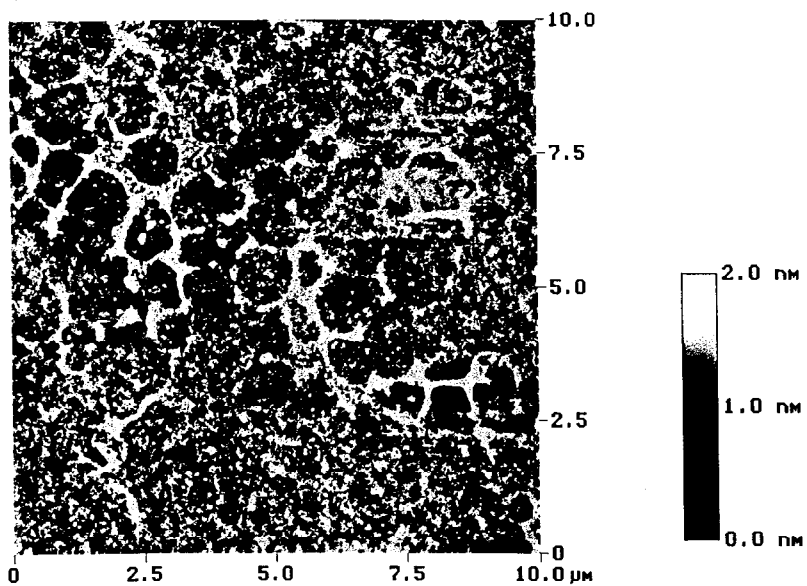


Figure MH.3.0.10: 10 μ m scan, multilayer-coated Hoya ULE wafer no.3, center. MSFR = 0.39nm rms. The ridges, which were likely caused by the underlying defects, were excluded from the roughness calculation.

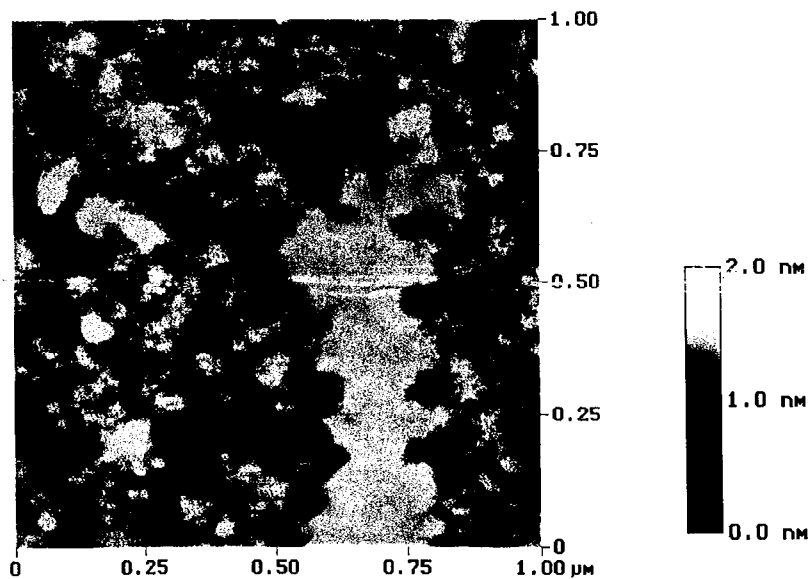


Figure MH.3.0.1: 1 μ m scan, multilayer-coated Hoya ULE wafer no.3, center. HSFR = 0.27nm rms. The ridge was excluded from the roughness calculation.

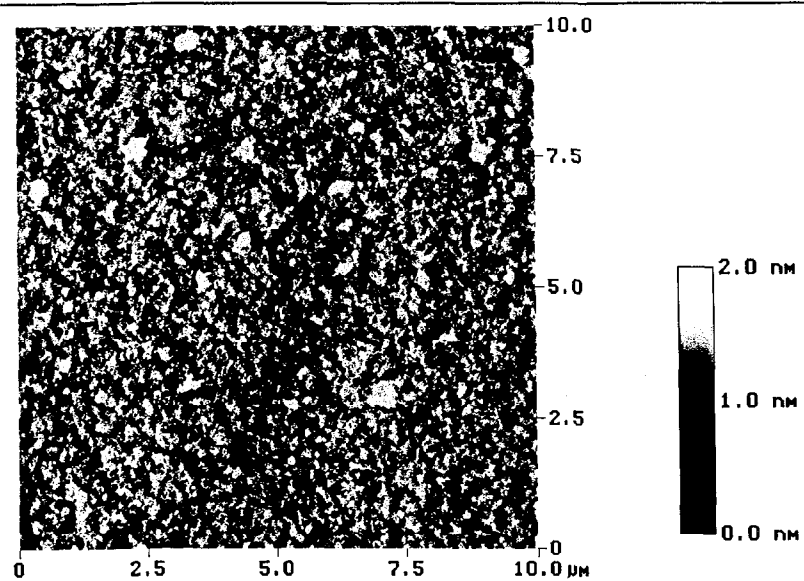


Figure MH.3.80.10: 10μm scan, multilayer-coated Hoya ULE wafer no.3, center. MSFR = 0.29nm rms. The discrete defects were excluded from the roughness calculation.

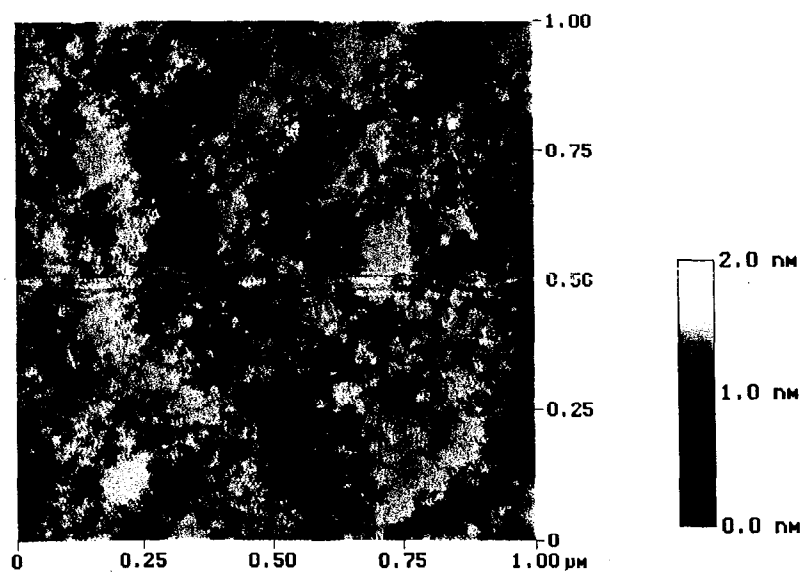
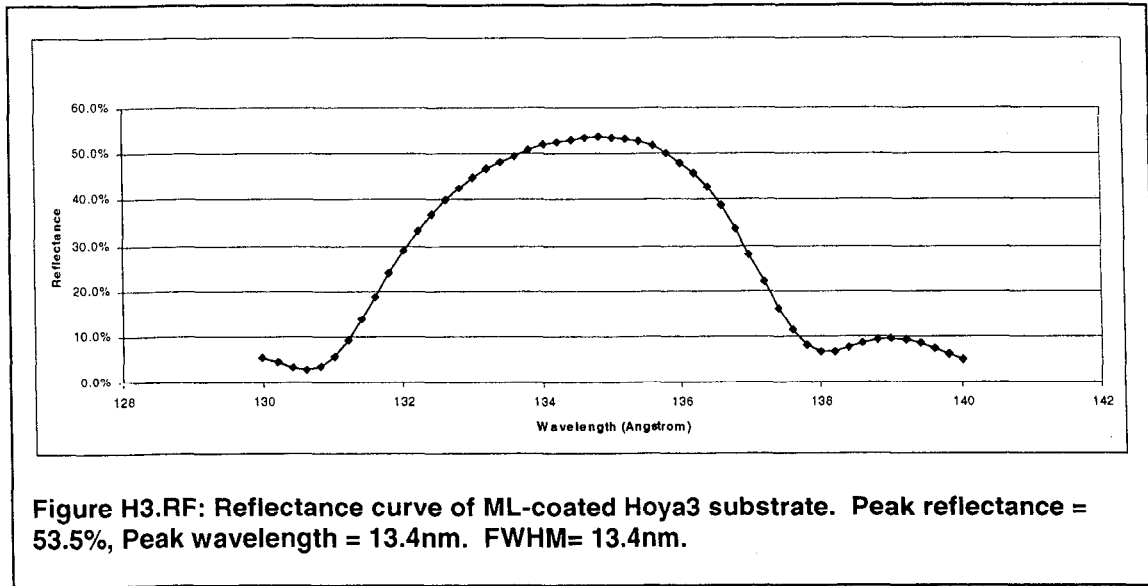


Figure MH.3.80.1: 1μm scan, multilayer-coated Hoya ULE wafer no.3, 80mm from center. HSFR = 0.34nm rms. The discrete defects were excluded from the roughness calculation.



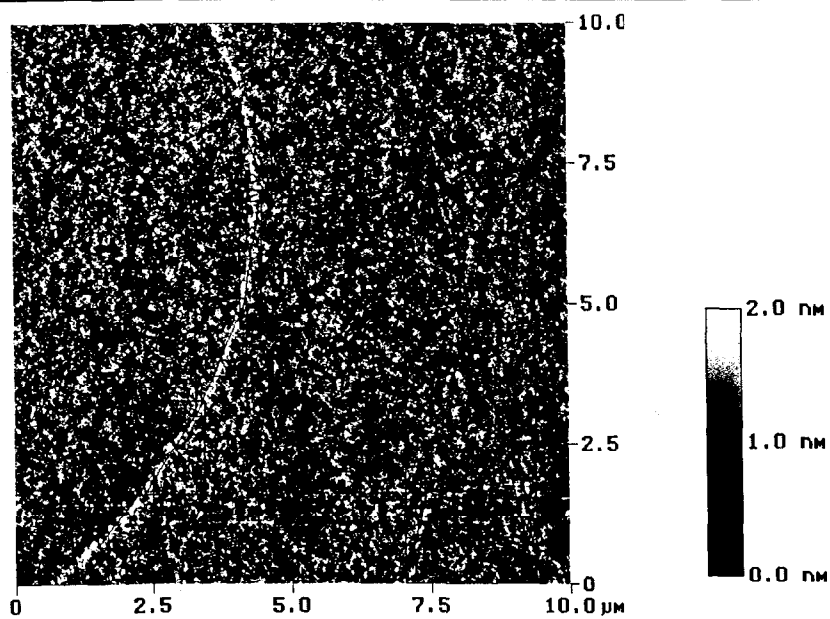


Figure H.4.0.10: 10μm scan, Hoya ULE wafer no.4, center. MSFR = 0.33 rms. The ridges on this surface are 2 to 3nm in height have not observed in other samples.

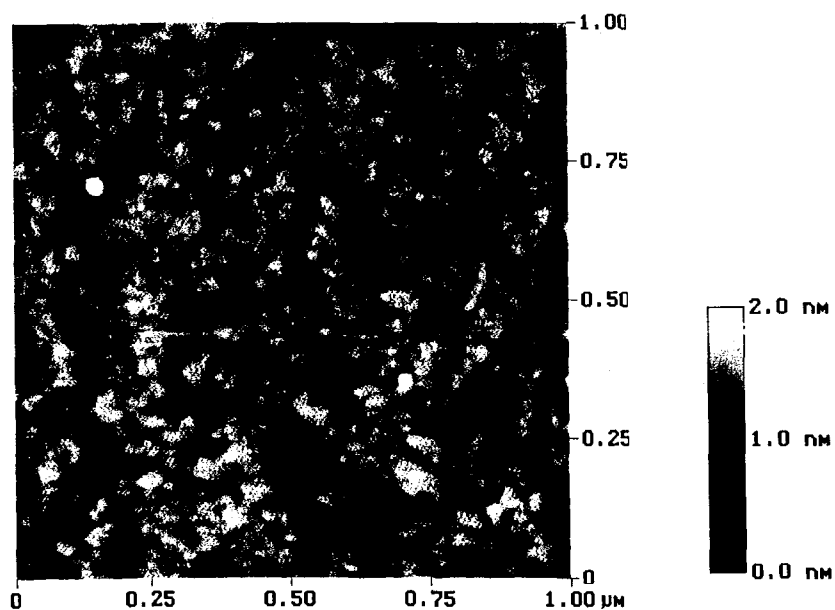


Figure H.4.0.1: 1μm scan, Hoya ULE wafer no.4, center. HSFR = 0.29nm rms. The defects were excluded from the roughness calculation.

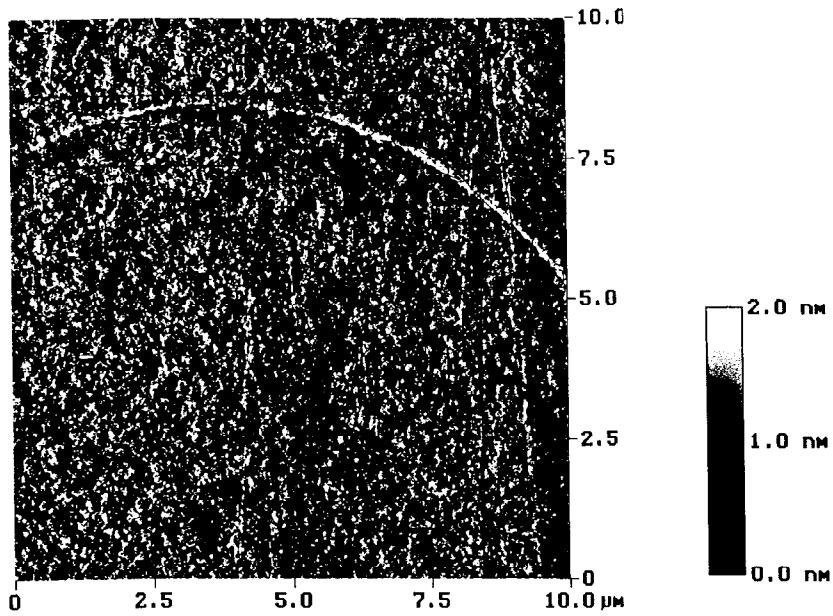


Figure H.4.80.10: 10μm scan, Hoya ULE wafer no.4, 80mm from center. MSFR = 0.38nm rms.

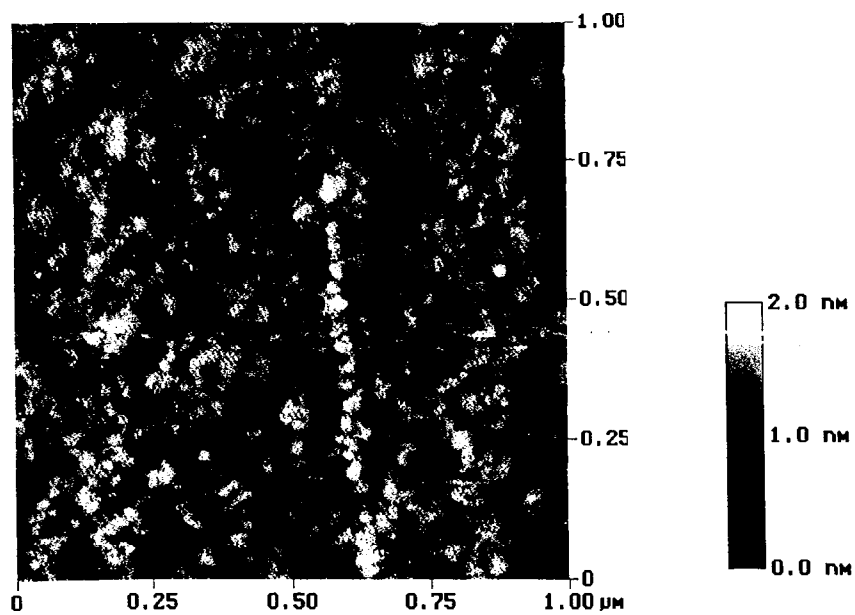


Figure H.4.80.1: 1μm scan, Hoya ULE wafer no.4, 80mm from center. HSFR = 0.29nm rms.

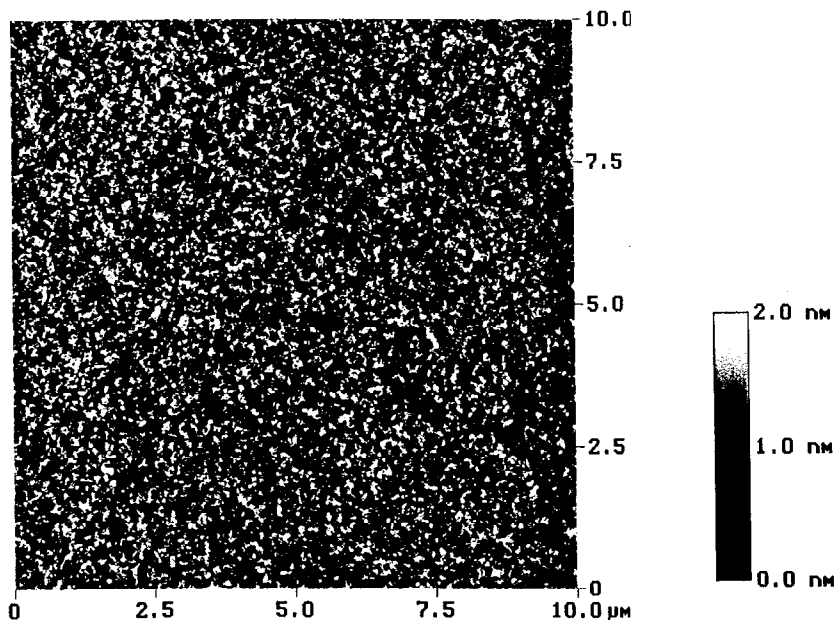


Figure MH.4.0.10: 10μm scan, multilayer-coated Hoya ULE wafer no.4, center. MSFR = 0.34nm rms.

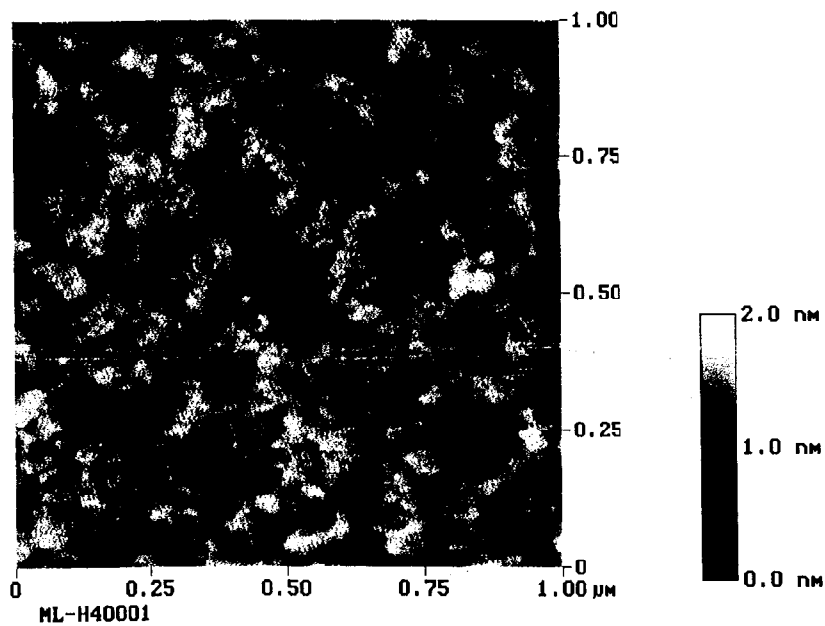


Figure MH.4.0.1: 1μm scan, multilayer-coated Hoya ULE wafer no.4, center. HSFR = 0.30nm rms.

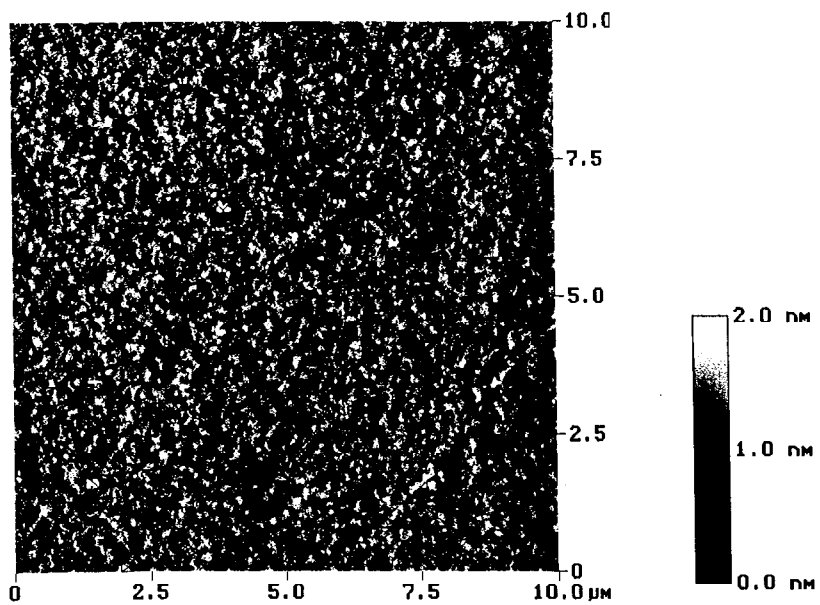


Figure MH.4.80.10: 10μm scan, multilayer-coated Hoya ULE wafer no.4, center. MSFR = 0.27nm rms.

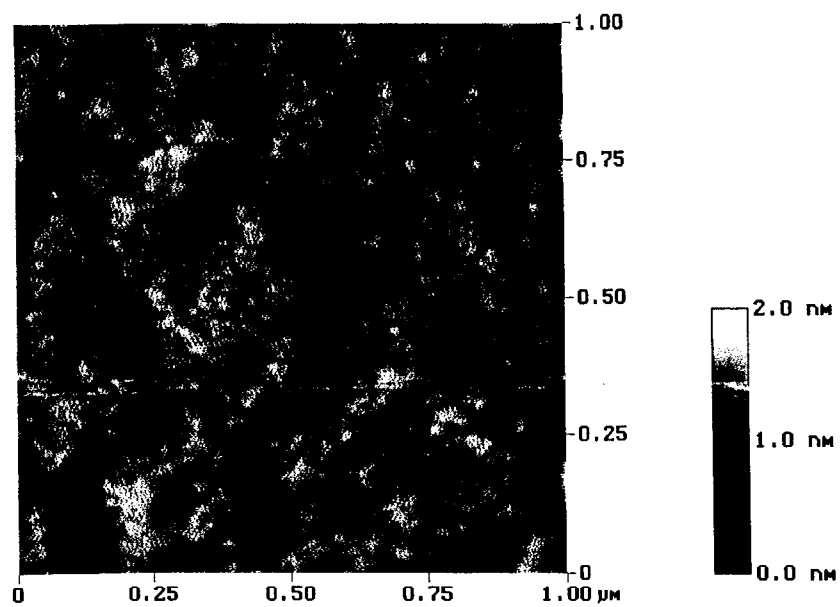


Figure MH.4.80.1: 1μm scan, multilayer-coated Hoya ULE wafer no.4, 80mm from center. HSFR = 0.23nm rms.

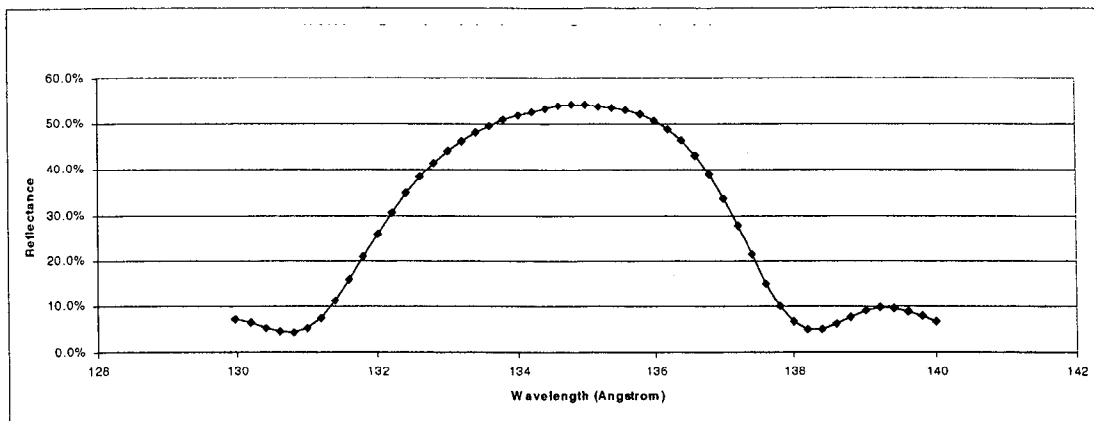


Figure H4.RF: Reflectance curve of ML-coated Hoya 4 substrate. Peak reflectance = 56.7%, Peak wavelength = 13.4nm.

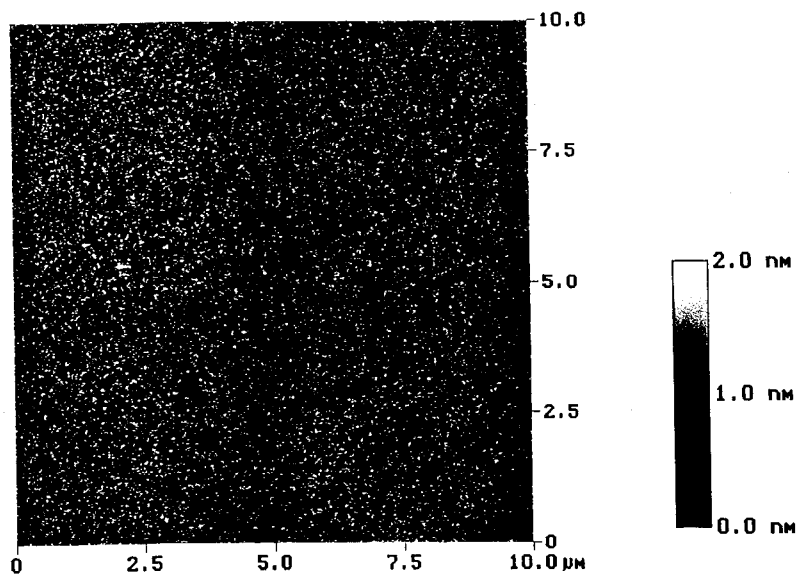


Figure G1.0.10: 10μm scan, GO ULE wafer no.1, center. MSFR = 0.19nm rms.

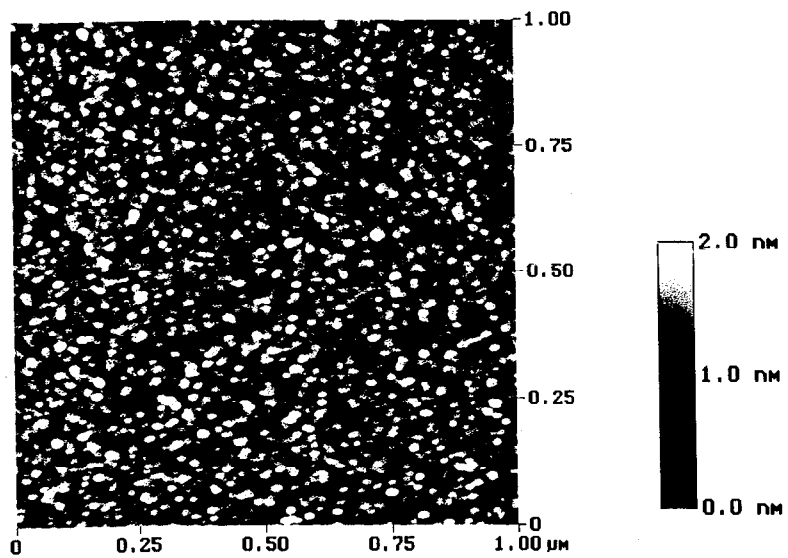


Figure G1.0.1: 1μm scan, GO ULE wafer no.1, center. HSFR = 0.38nm rms.

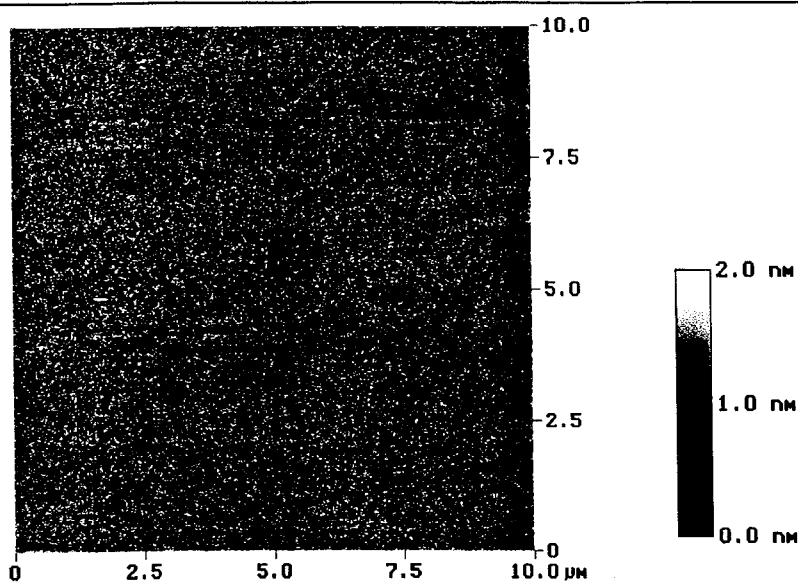


Figure G1.80.10: 10μm scan, GO ULE wafer no.1, 80mm from center. MSFR = 0.29nm rms. The boxed areas denote sleeves which have been excluded from the calculation of roughness.

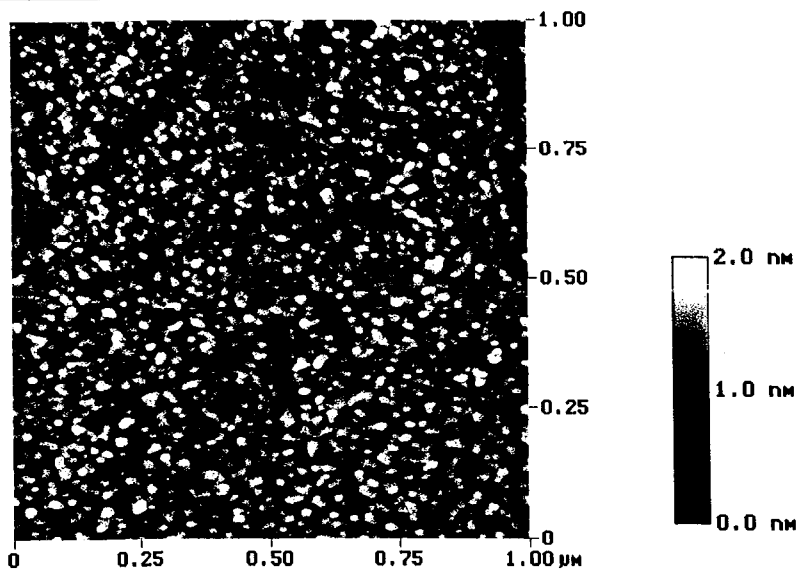


Figure G1.80.1: 1μm scan, GO ULE wafer no.1, 80mm from center. HSFR = 0.38nm rms.

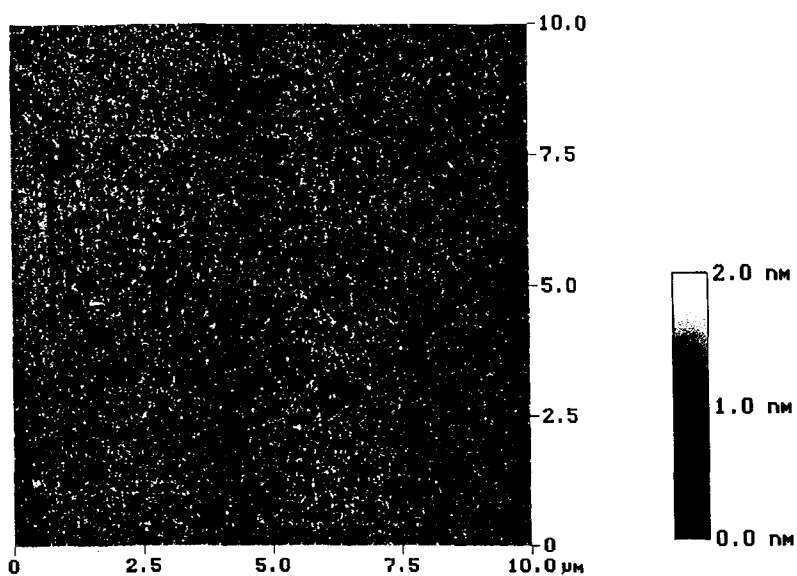


Figure MG1.0.10: 10μm scan, multilayer-coated GO ULE wafer no.1, center. MSFR = 0.34nm rms.

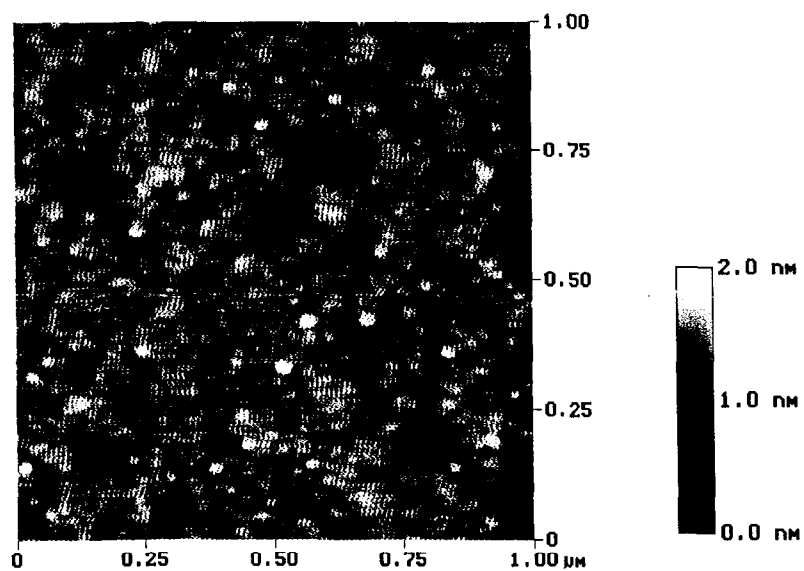


Figure MG1.0.1: 1μm scan, multilayer-coated GO ULE wafer no.1, center. HSFR = 0.30nm rms.

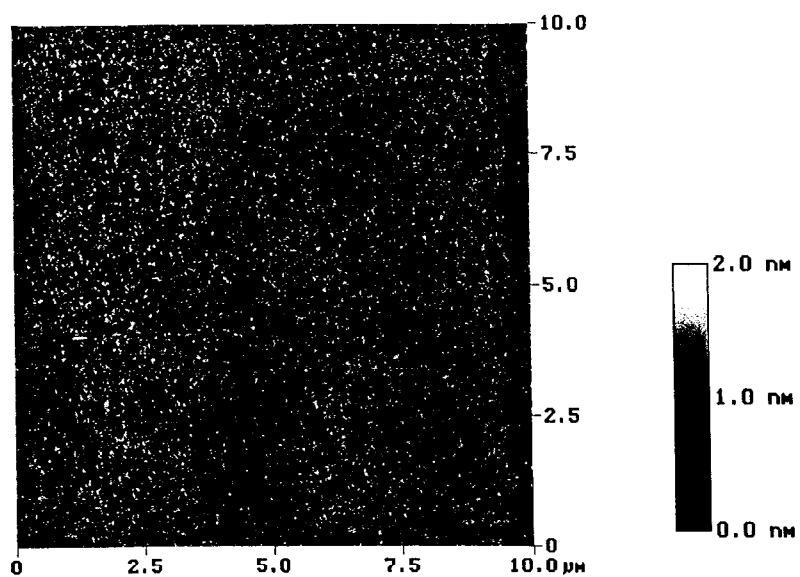


Figure MG1.80.10: 10 μ m scan, multilayer-coated GO ULE wafer no.1, 80mm from center. MSFR = 0.27nm rms.

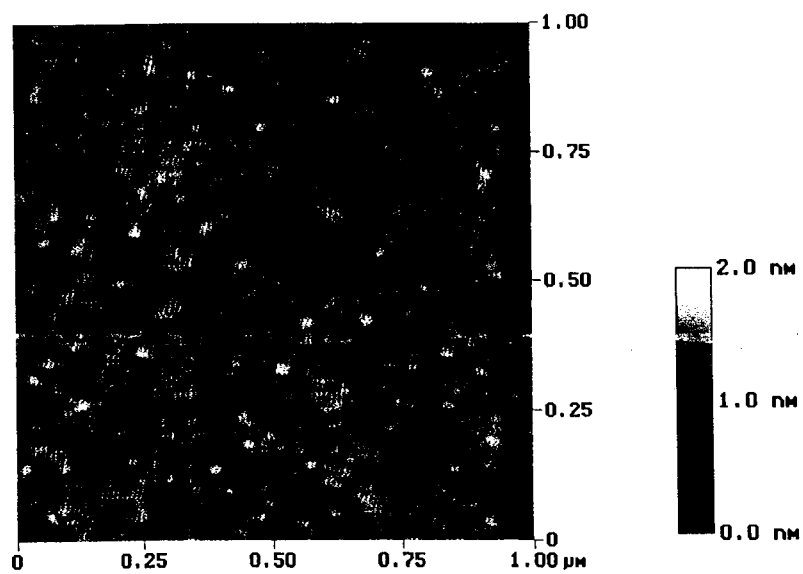


Figure MG1.80.1: 1 μ m scan, multilayer-coated GO ULE wafer no.1, 80mm from center. MSFR = 0.23nm rms.

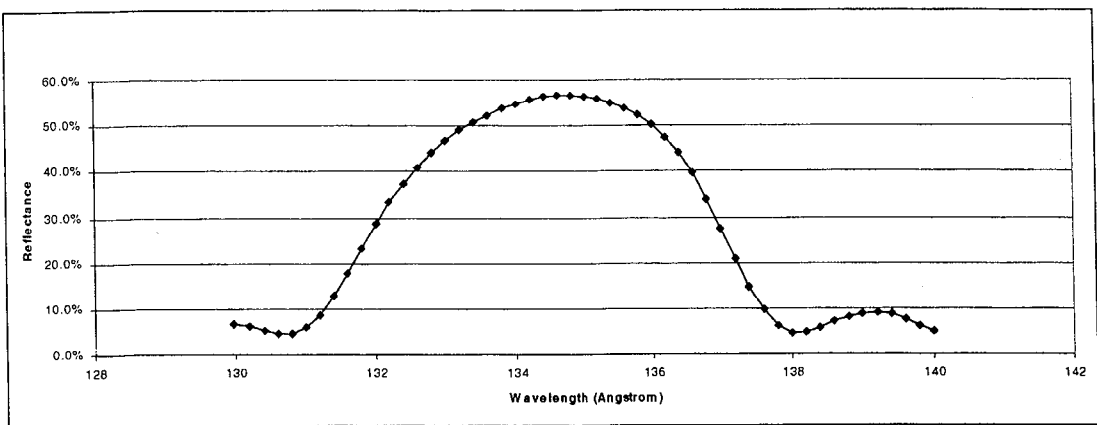


Figure G1.RF: Reflectance curve of ML-coated GO1 substrate. Peak reflectance = 56.7%, Peak wavelength = 13.4nm.

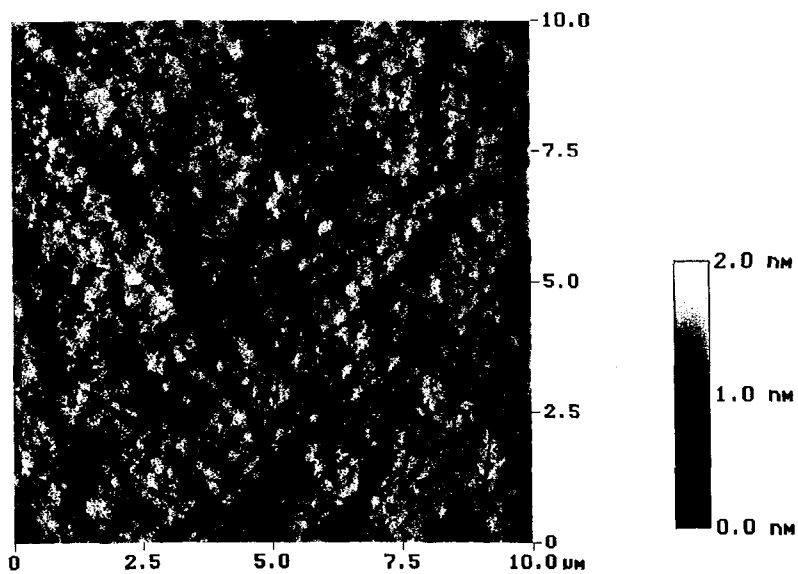


Figure R1.0.10: 10μm scan, Rodel ULE wafer no.1, center. MSFR = 0.21nm rms. The polishing streaks on this surface are on the average 0.37nm deep and 280nm width at the top.

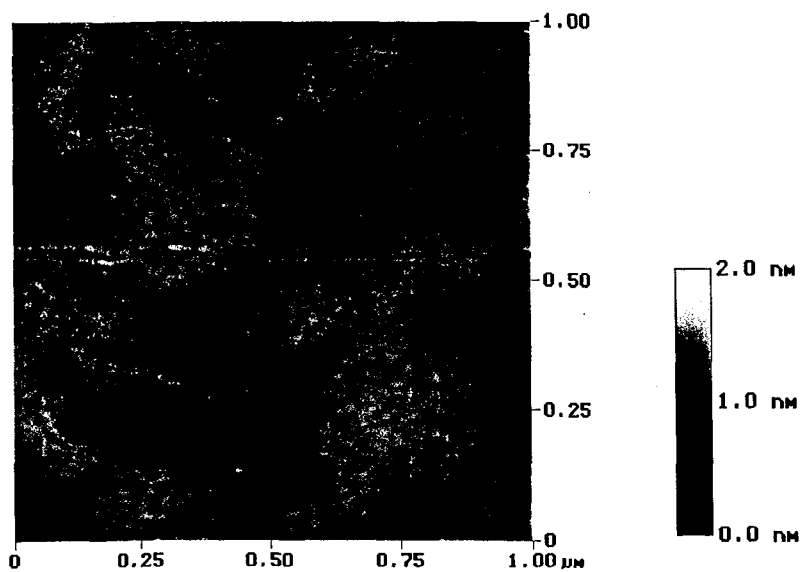


Figure R1.0.1: 1μm scan, Rodel ULE wafer no.1, center. HSFR = 0.15nm rms.

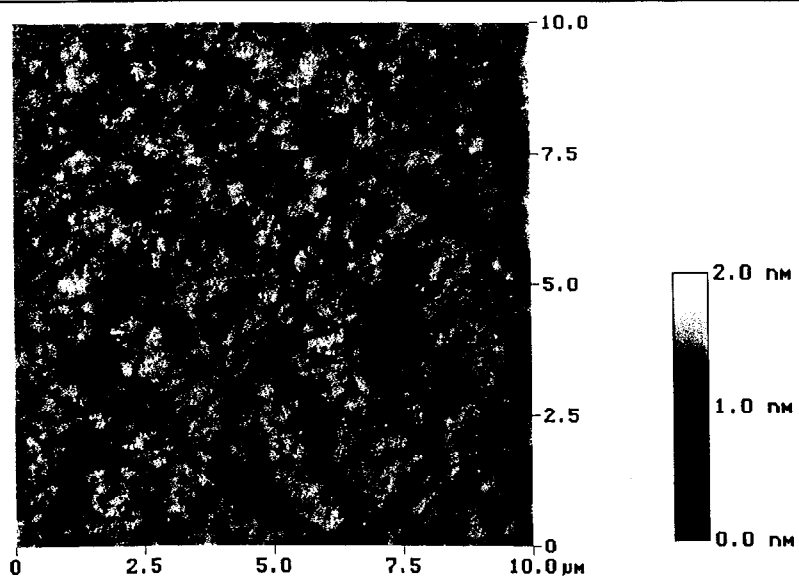


Figure R1.80.10: 10μm scan, Rodel ULE wafer no.1, 80mm from center. MSFR = 0.19nm rms.

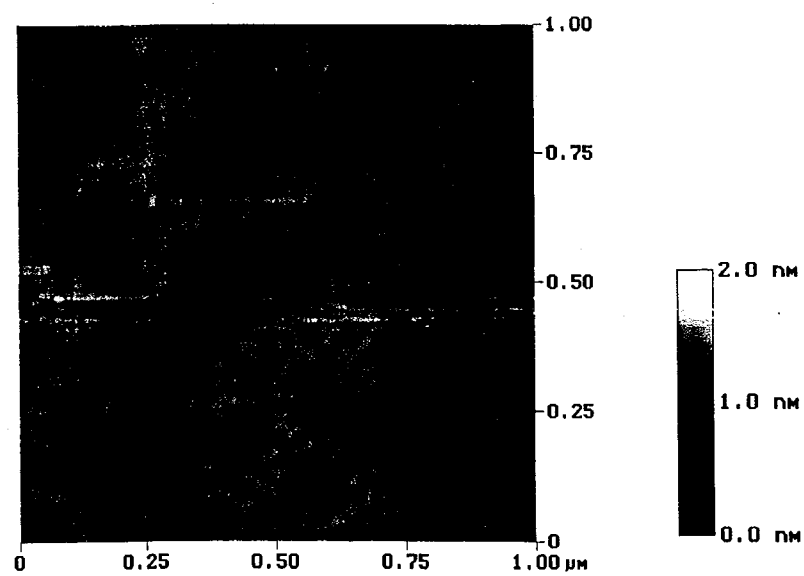


Figure R1.80.1: 1μm scan, 1μm scan, Rodel ULE wafer no.1, 80mm from center. HSFR = 0.13nm rms.

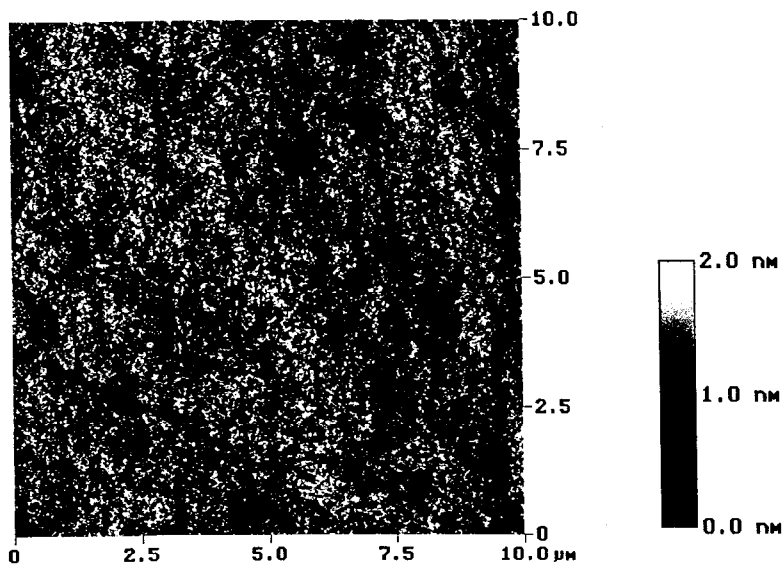


Figure MR1.0.10: 10 μm scan, multilayer-coated Rodel ULE wafer no.1, center. MSFR = 0.30nm rms. The sleeves on this surface have been further smoothed by the ML coating process. They are not printable.

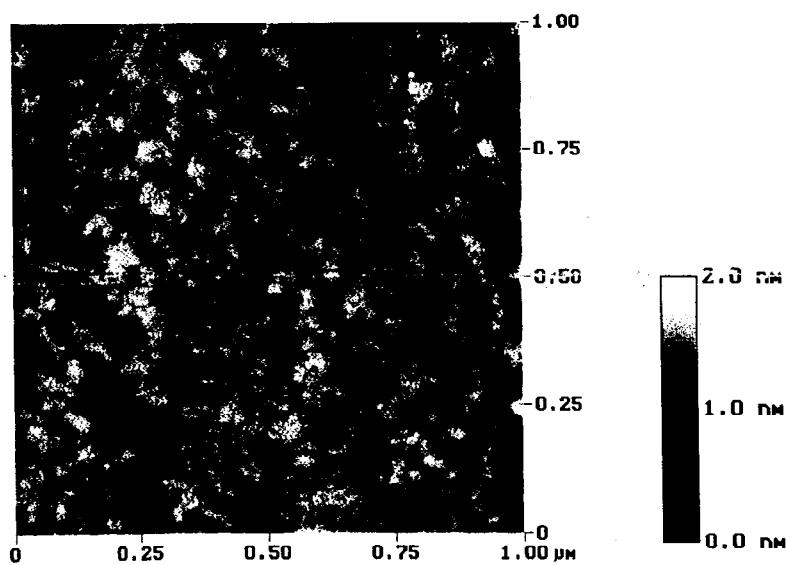


Figure MR1.0.1: 1 μm scan, multilayer-coated Rodel ULE wafer no.1, center. HSFR = 0.26nm rms.

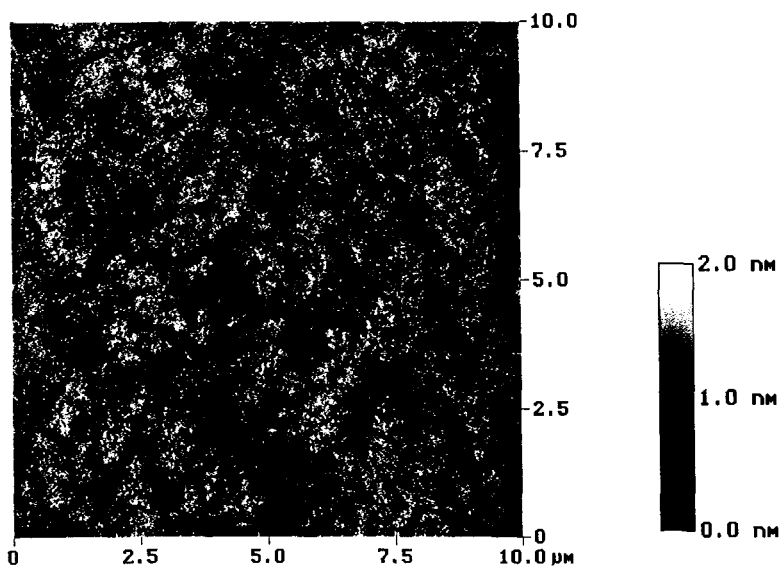


Figure MR1.80.10: 10 μ m scan, multilayer-coated Rodel ULE wafer no.1, 80mm from center. MSFR = 0.22nm rms. The sleeks on this surface have been further smoothed by the ML coating process. They are not printable.

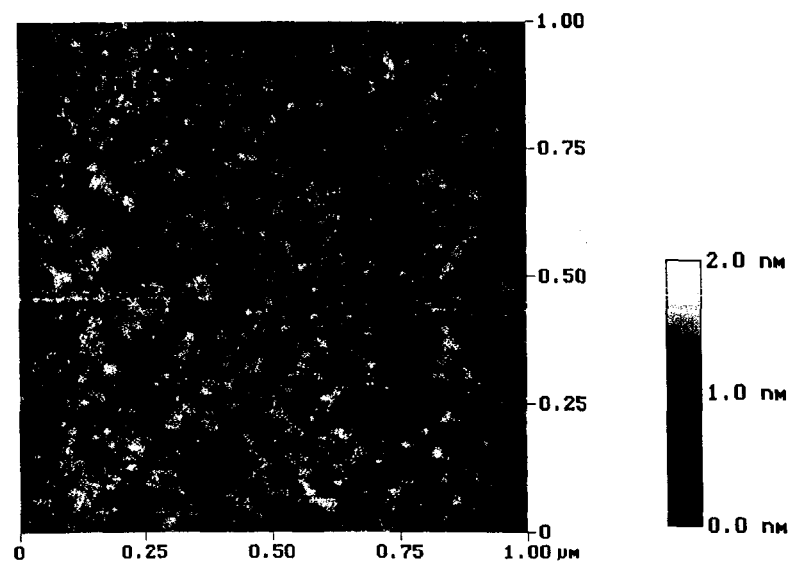
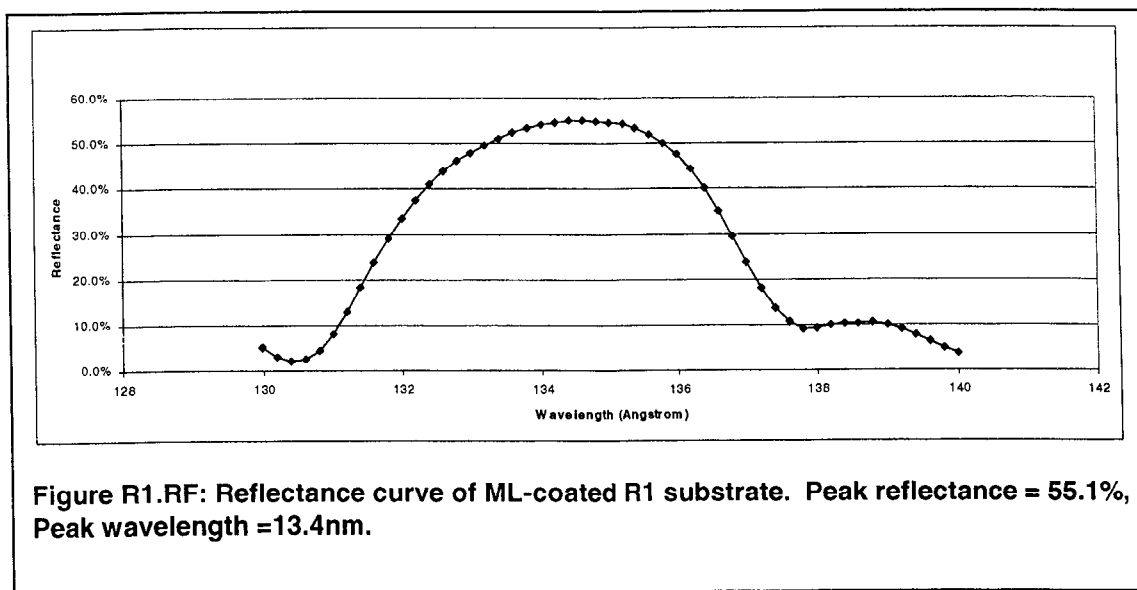


Figure MR1.80.1: 1 μ m scan, multilayer-coated Rodel ULE wafer no.1, 80mm from center. HSFR = 0.16nm rms.



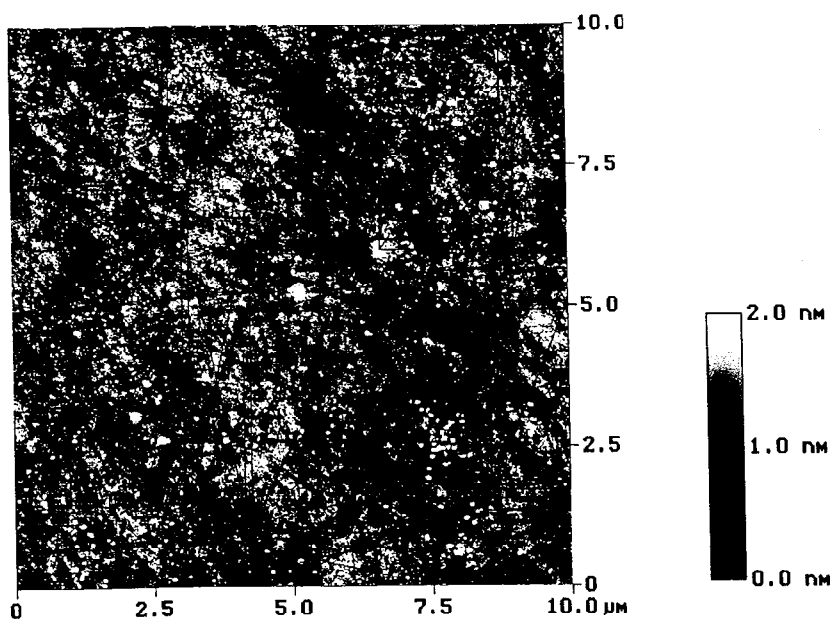


Figure R2.0.10: 10μm scan, multilayer-coated Rodel ULE wafer no.2, center. MSFR = 0.47nm rms. *

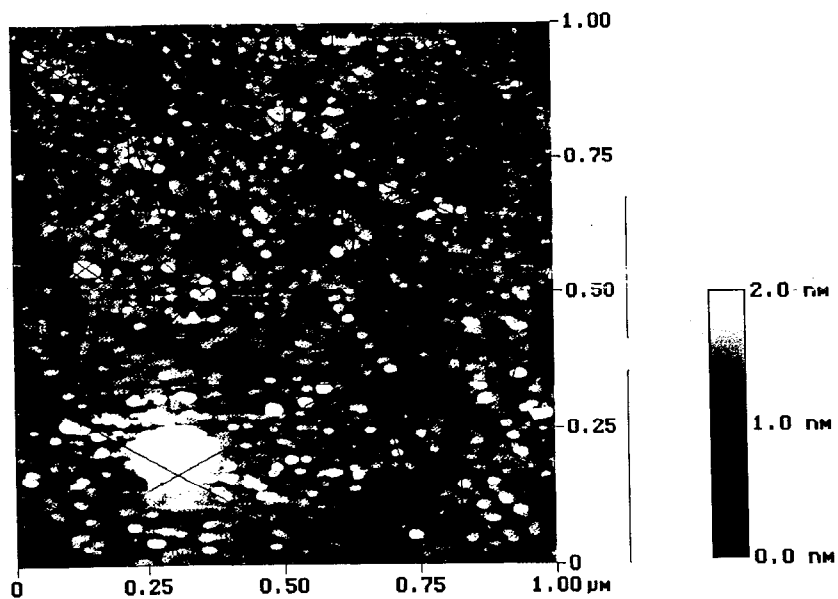


Figure R2.0.1: 1μm scan, Rodel ULE wafer no.2, center. HSFR = 0.33nm rms. *

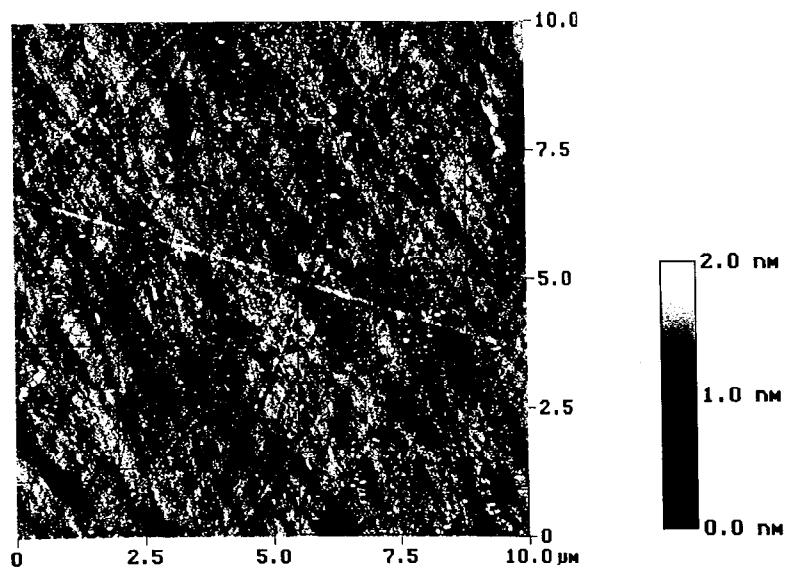


Figure R2.80.10: 10μm scan, Rodel ULE wafer no.2, 80mm from center. MSFR = 0.65nm rms. *

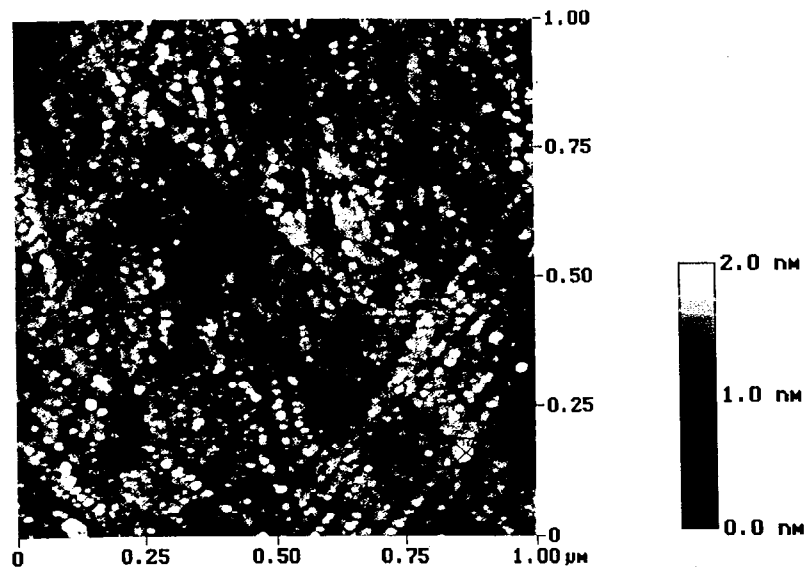


Figure R2.80.1: 1μm scan, Rodel ULE wafer no.2, 80mm from center. HSFR = 0.44nm rms. *

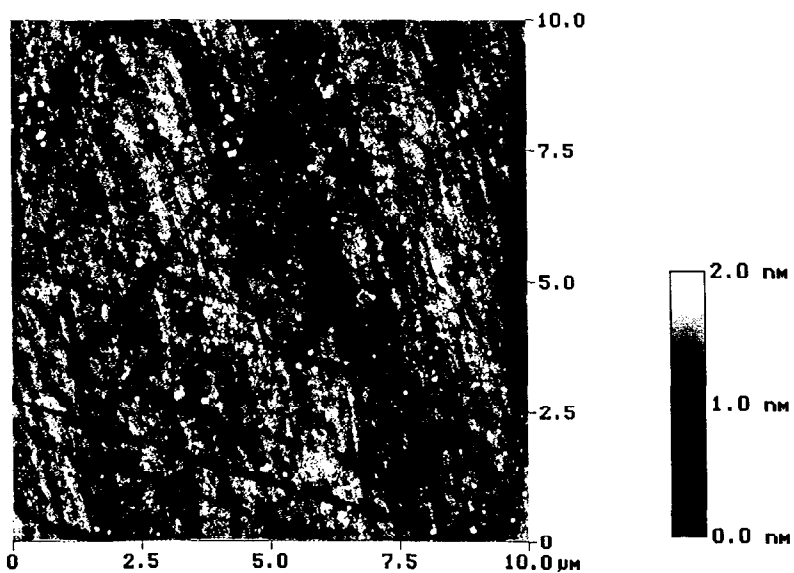


Figure MR2.0.10: 10μm scan, multilayer-coated Rodel ULE wafer no.2, center. MSFR = 0.42nm rms.*

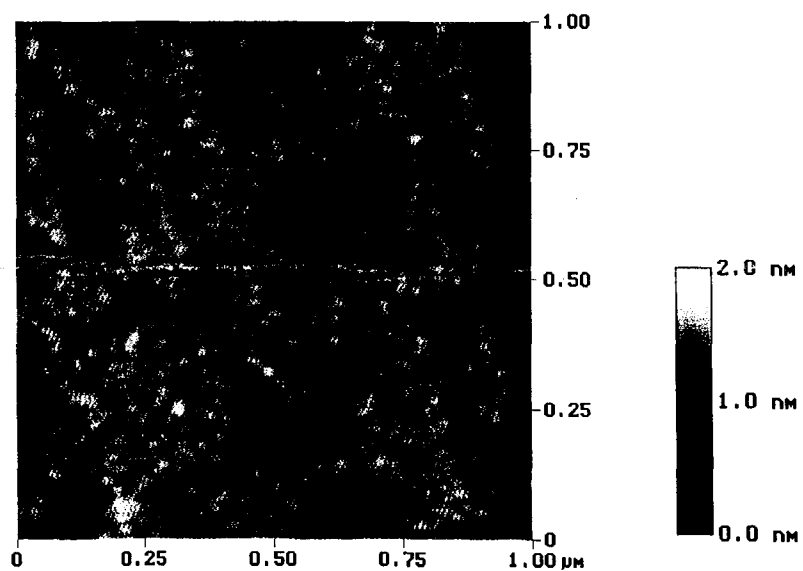


Figure MR2.0.1: 1μm scan, multilayer-coated Rodel ULE wafer no.2, center. HSFR = 0.21nm rms.*

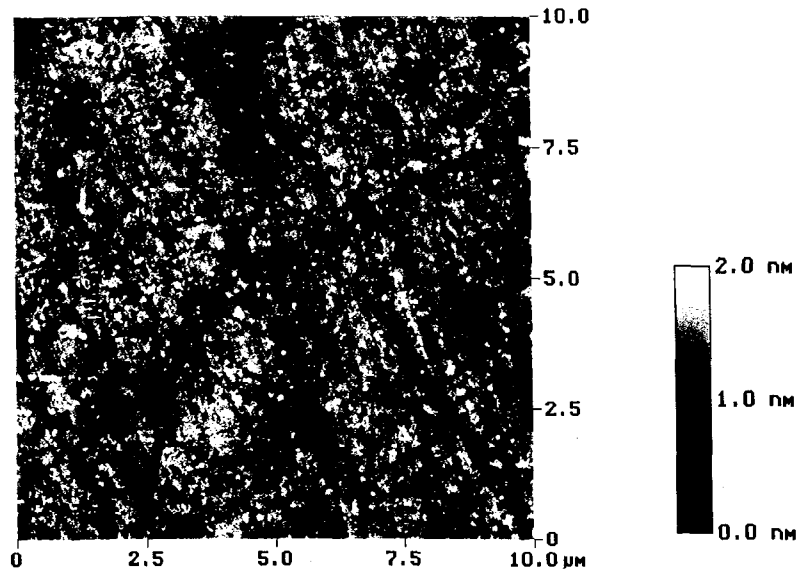


Figure MR2.80.10: 10μm scan, multilayer-coated Rodel ULE wafer no.2, 80mm from center. MSFR = 0.42nm rms.*

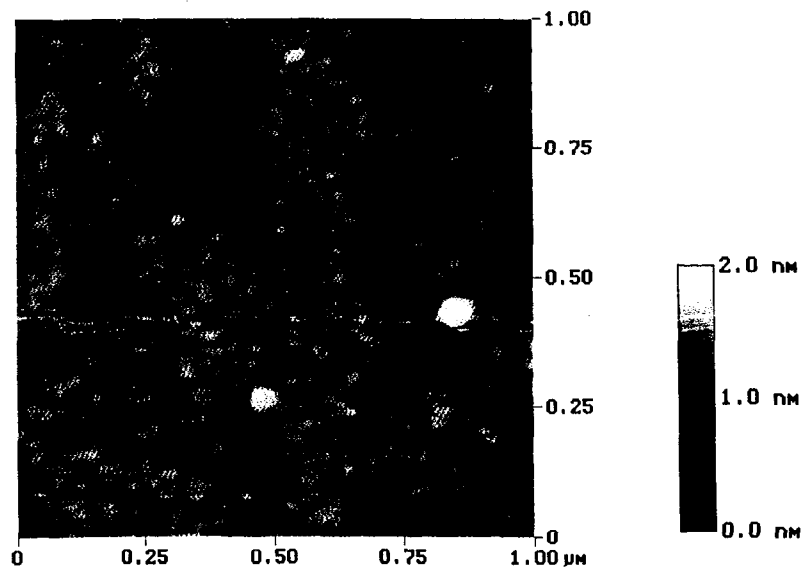


Figure MR4.80.1: 1μm scan, multilayer-coated Rodel ULE wafer no.2, 80mm from center. HSFR = 0.19nm rms.*

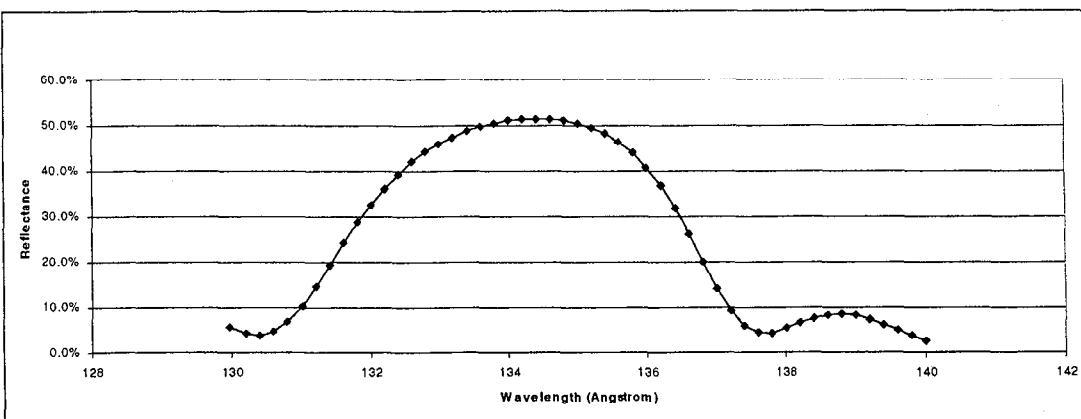


Figure R2.RF: Reflectance curve of ML-coated R2 substrate. Peak reflectance = 51.5%, Peak wavelength =13.4nm.

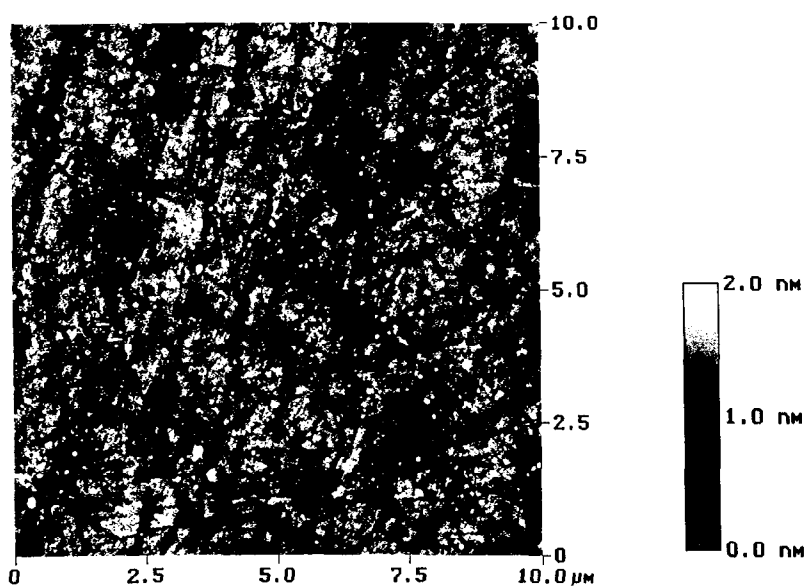


Figure MR4.0.10: 10μm scan, multilayer-coated Rodel ULE wafer no.4, center. MSFR = 0.45nm rms. *

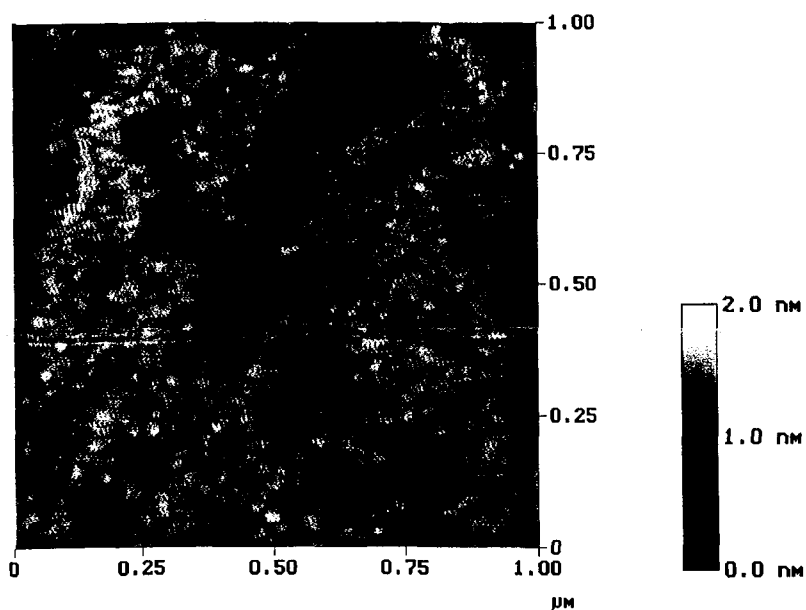


Figure MR4.0.1: 1μm scan, multilayer-coated Rodel ULE wafer no.4, center. HSFR = 0.32nm rms. *

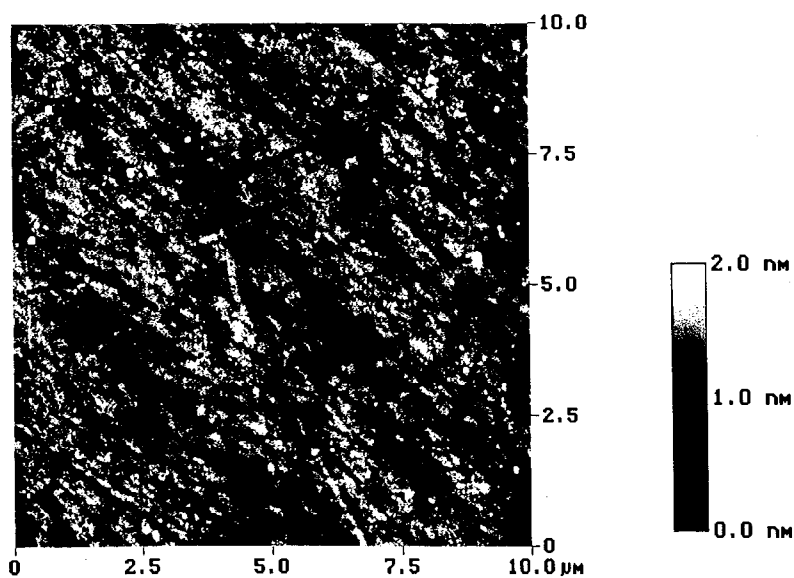


Figure MR4.80.10: 10μm scan, multilayer-coated Rodel ULE wafer no.4, 80mm from center. MSFR = 0.39nm rms.*

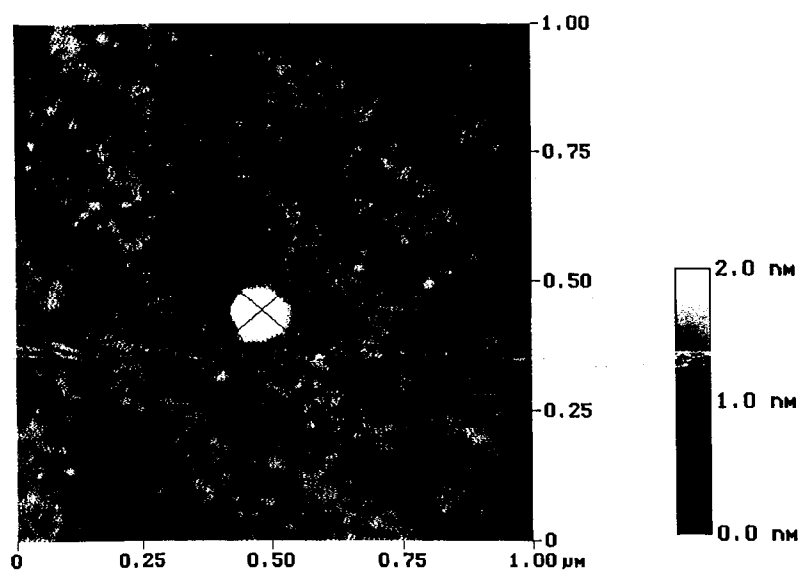


Figure MR4.80.1: 1μm scan, multilayer-coated Rodel ULE wafer no.4, 80mm from center. HSFR = 0.20nm rms.*

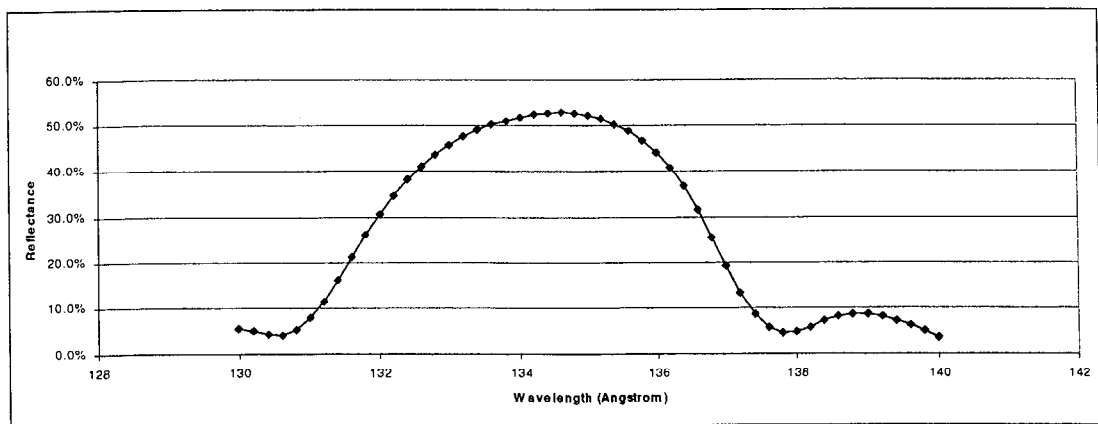


Figure R4.RF.80.10: Reflectance curve of ML-coated R4 substrate. Peak reflectance = 52.8%, Peak wavelength = 13.5nm.